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EXPERIMENT TEST OF THE RELIABILITY OF COMPUTER SYSTEMS OF INTEGRATED MODULAR AVIONICS

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Introduction

The task of designing advanced computing systems in the class of integrated modular avionics (IMA) structures is urgent. The development of IMA computing modules requires the development of test schemes and software specialized for IMA class products, both in the process of operation on the aircraft and in the process of production at the factory. Unification of IMA modules will allow to build an automated workplace for product inspection, which has increased rates of unification and standardization of design solutions.

Object of research: on-board digital computing system developed in accordance with the IMA concept.

Subject of research: methods and means of control of the aircraft of IMA, used during the flight of the aircraft and during the production of the aircraft and its functional elements at the factory.

The purpose of the study: is to assess the reliability of IMA computing structures for different configurations of hardware. As well as in the development of means of control of the aircraft IMA, which provide verification of the computer system and functional elements (modules) included in it, in the process of flight of the aircraft and in the process of manufacturing the aircraft at the factory.

To achieve the goal of the study it is necessary to solve the following tasks:

- to single out the principles of construction of the IMA aircraft and its functional elements (modules);
- to develop methods and means of control of IMA computer systems;
- evaluate the reliability of IMA computing structures for different hardware configurations;
- to develop a scheme of a unified automated inspection workplace, which is used to control the functional elements of the aircraft at the factory.

Literature analysis and problem statement

Aviation computers of the IMA class are [1-2] multiprocessor multi-module computing systems, which include the following unified functional modules: computing module, graphics module, I/O module, mass memory module. The supply voltage to the functional module provides a voltage module.

On the basis of the functional module are designed [3-4]: on-board digital computer system, on-board graphics station, on-board interface station, on-board cartographic information system and a number of other products of the aviation industry that implement on-board computing functions.

The internal structure of the computer [5-10], which is considered as the communication scheme of the functional module in the product, and the λ-characteristics of the reliability of the element base of the functional module included in the product are essential for assessing the reliability of IMA class computers.

Thus, there is a problem to assess the reliability of the product, which is carried out by analytical expression for the probability P(t) of trouble-free operation of the product and the construction of a family of graphs of this probability at a given time interval. The time interval characterizes the expected time of continuous operation of the product in operation [11-15].

Among the many possible configurations of on-board digital computing systems, a distinction is made between fully connected

(when each of the network subscribers is directly connected to all other subscribers via separate physical communication lines) and non-fully connected networks. Not fully connected configurations are distinguished: mesh topology, ring topology, star topology, and "shared bus" configuration. Examples of existing products of computing systems of the IMA class are as follows: multiprocessor computing complexes (MPVK) developed by ZAO NPP Aviation and Marine Electronics (St. Petersburg); "Basis 5.0" developed by JSC "Scientific and Design Bureau of Computing Systems" (Taganrog), etc.

According to the technical documentation, the multiprocessor computing complex is designed for multichannel digital processing of large information flows in real time and can be used both as an autonomous onboard computing system and for building cluster supercomputers. The structure of multiprocessor computing systems includes:

- up to 8 modules of digital processor signals, which are dual-processor devices (one processor is installed on the main board, the second - on an additional mezzanine module);
- central processor module;
- backplane cross-board of intermodular connections;
- power supply module.

To organize intrasystem interaction, a standard interface is used - the CompactPCI system bus (PICMG 2.0 D3.0) and specialized interfaces. The level of intersystem interaction is represented by:

- the system level, which ensures the organization of information interaction between the signals of the digital processor module and the central processor module via the standard CompactPCI bus interface;
- the level of information interaction of the digital processor module, which provides high-speed data exchange between the digital processor signal modules via a specialized interface;
- the level of interprocessor communication, which provides data exchange between the main and mezzanine processors in the digital processor signals module.

Materials and methods

In fig. 1 and shows a diagram of the internal communication functional module in a computer system divided into two identical sub-systems, each of which involves four functional modules and one module of non-volatile memory. As part of the aircraft object subsystems reserve each other. If one of the constructive-functional modules in the subsystem fails, the whole sub-system is considered faulty, the functions of the calculator are performed by the backup subsystem [16-20].

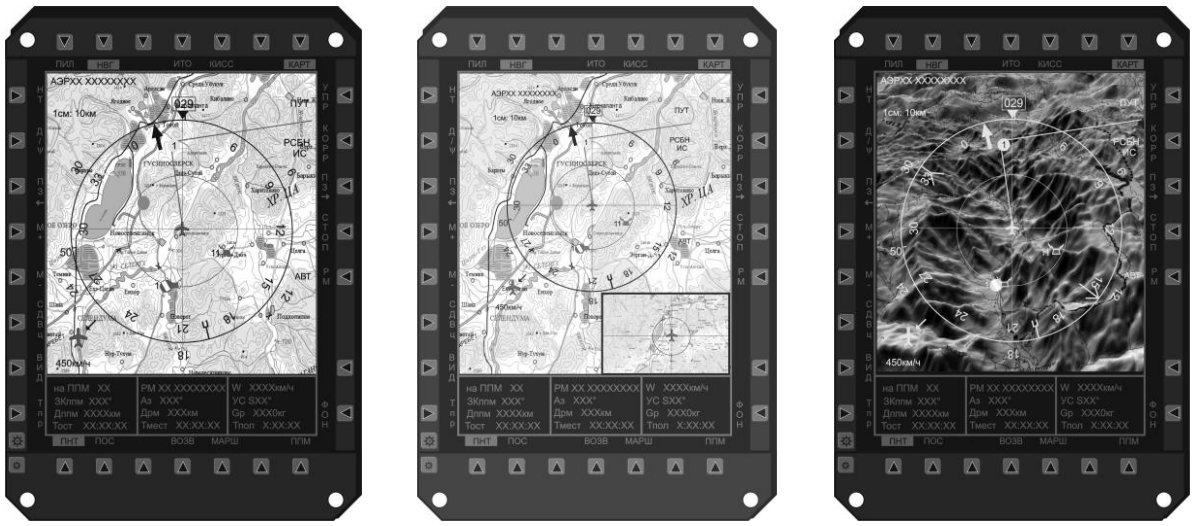
Thus, four tasks of formation and reflection were realized:

1. The formation of a video image for a two-dimensional digital terrain map (CCM), which changes dynamically with the output of the image on the indicator, the screen resolution of which is 1024x768 pixels; the image was formed on the basis of data stored in the ROM of processors (Fig.1a).

2. The formation of a single video image, which consists of two two-dimensional images of a digital map of the terrain based on dynamically changing data stored in the ROM processors, and the output of this image on a screen with a total screen size of 1024x1024 pixels with different scales: 1:1 km and 1: 4 km (Fig.1b).

3. The formation of a video image of a three-dimensional surface that changes dynamically with calculations based on the mathematical formula of the surface itself and the coordinates of the chromaticity of the pixels for the resulting surface; display of this surface on the indicator screen;

4. The formation of a video image of the three-dimensional relief of the CCM on the basis of data stored in the ROM of the processor (height matrix) (Fig.1c).



a) b) c)

Fig. 1. Examples of displaying the terrain map on the indicator:

a) two-dimensional display of the terrain map,

b) two-dimensional display of the terrain map with the function "picture in picture",

c) three-dimensional display of the terrain map.

In task 1 (two-dimensional display of the terrain map), one of the processors (CPU2) selects data from the ROM2, which contains the terrain map, and sets the positioning point of the aircraft, using data about the current location of the object, which can be obtained from satellite or inertial navigation systems.

This processor (CPU2) performs processing of the map of the area into data that is the absolute coordinates of the indicator screen with the possibility of implementing support for rotating the map (in the polar coordinate system). Another processor (CPU1) provides the formation of the final representation of the video image. The result of CPU2 determines the color of each pixel.

The work of the module is represented by the following stages, which are carried out simultaneously:

- one processor (CPU2) implements the specified operation and outputs the result of this action to another processor (CPU1), which writes the incoming data to its RAM;
- another processor (CPU1) implements the specified operation (simultaneously with the implementation of the functions of the graphics controller in the controller of shared access to memory), then writes the received data to the RAM bank with shared access;
- the memory shared controller cleans (resets) the RAM bank and records data from another RAM bank (taking into account the data obtained at the previous stage) into the RAM output buffer of the third public access RAM bank;
- the test is performed against the background of the general task.

In task 2, a similar information processing is performed to form two video images with different scales of the terrain map.

In task 3, CPU1 performs all the actions for image formation, and CPU2 is not used.

The operation of the module is represented by the following steps, which are carried out simultaneously:

- the processor (CPU1) implements the specified operation (simultaneously with the implementation of the functions of the graphics controller in the controller of shared access to memory), then writes the received data to the RAM bank with shared access;
- the memory shared controller cleans (resets) the RAM bank and records data from

another RAM bank (taking into account the data obtained at the previous stage) in the RAM output buffer of the third public access RAM bank;

- the test is performed against the background of the general task.

In task 4, CPU1 performs all the actions for image formation, and CPU2 is not used. CPU1 selects the height matrix from its ROM, then processes this data and obtains their vector format (triangular primitives), calculates the color and hue of the displayed components of the terrain map and translates the vector image format into a pixel format suitable for panel display. indicator.

The operation of the module is represented by the following steps, which are carried out simultaneously:

- the processor (CPU1) implements the specified operation (simultaneously with the implementation of the functions of the graphics controller in the controller of shared access to memory), then writes the received data to the RAM bank with shared access;
- the memory shared controller cleans (resets) the RAM bank and records data from another RAM bank (taking into account the data obtained at the previous stage) into the RAM output buffer of the third public access RAM bank;
- the test is performed against the background of the general task.

Implemented two hardware modes.

In the first hardware mode the support of the following graphic functions is carried out: memory clearing, copying of the information in video RAM, function of the pixel processor with realization of formation of a primitive "Line". The first processor (CPU1) calculates the coordinates of the boundaries of elementary objects and writes them to the RAM or transmits them to the second processor (CPU2) to form primitives such as "Polygon". The first processor also performs the formation of characters and letters.

In the second hardware mode, the following graphical functions are supported: memory clearing, copying information to video RAM, pixel processor function with the implementation of the formation of a horizontal line between two points, with the implementation of the function of forming colors and shades; line processor with the ability to form a primitive type "Laman line".

The first processor performs processing of elementary objects at a minimum and writes data to the memory of the processor lines, where the information is issued to the controller hardware formation of lines, and then to one of the banks of RAM when forming a primitive "Line" or a pixel processor when forming other primitives. The first processor also produces letters and symbols.

Estimation of productivity of system of display of geographical information data in a mode of execution of the functional software and tests is realized by measurement of frequency of updating of frames of video image at display of a digital map of district. The results are summarized in table. 1.

Some variance in the implementation of the first and second tasks in both modes is determined by the complexity of the terrain map and the number of layers displayed on the screen.

Table 1. The results of the evaluation of system performance

Regime	**Problem**			
	1	2	3	4
1	4 – 9 Hz	5 – 12 Hz	3,5 Hz	0,29 Hz
2	7,5 – 10 Hz	5 – 12 Hz	5,9 Hz	0,36 Hz

The small increase in system performance during the transition from the first hardware mode to the second hardware mode is explained by the fact that the implementation of the function of calculating colors and shades, which adds additional operation

"read-modification" (calculation of coordinates and color), thus the number of interactions with RAM increases approximately twice and additional calculations are performed.

After the manufacture of the product at the stage of preliminary or interdepartmental tests, the conformity of the product to the requirements of the technical task on electromagnetic compatibility in the work with onboard equipment is assessed.

When conducting experiments to assess the levels of electromagnetic interference (interference emission) to be studied:

- measurement of the voltage of electromagnetic interference in the power supply wires of the product (forward and reverse);
- measurement of electromagnetic interference current in circuits and in signal circuits (communication cables);
- measurement of the electric field strength of the electromagnetic interference on different sides of the product.

When conducting experiments to assess the susceptibility of the product to electromagnetic interference (EMF) to be studied:

- resistance of the product to the influence of the magnetic field caused by the flow of alternating current in the wire-inductor;
- resistance of the product to the influence of the magnetic field of the sound frequency;
- resistance of the product to the impact on the connecting cables of the product of the electric field;
- resistance of the product to the impact on the connecting cables of the product of the fields of transients;
- resistance of the product to the impact on the power supply wires of the product of radio frequency electromagnetic interference;
- resistance of the product to the impact on the connecting cables of the product of radio frequency electromagnetic interference;
- resistance of the product to impact on the product and connecting cables of radio frequency radiation;
- resistance of the product to the impact on the power supply wires of the product of electromagnetic interference of sound frequencies.

To ensure the resistance of the product to external electromagnetic interference, the product uses specialized electroradiocomponents that are resistant to high levels of EMF; EMF-absorbing materials and coatings; structural elements of grounding of the product and elements of metallization of its parts.

In particular, to reduce the level of EMF emitted from harnesses and cables, the following measures are taken:

- shielding of circuits with pulse currents and the most important analog circuits with low dynamic range;
- mutual compensation of magnetic fluxes created by these circuits, due to the use of bifilar mounting;
- implementation of high-quality grounding of the shielding layer of harnesses and reduction of inductance during the metallization of the shielding layer of harnesses and cables;
- reduction of impedance of grounding busbars;
- reducing the area of the EMF radiation circuit by reducing the length of harnesses and cables;
- placement of harnesses and cables as close as possible to the grounded structural elements: chassis, block body, etc.;
- application of materials with frequency-dependent properties based on high-frequency ferrites for shielding power circuits, circuits with pulsed currents and the most important analog circuits with low dynamic range.

In terms of designing a multilayer printed circuit board to reduce the level of emitted EMF, the following rules must be followed:

- to increase the interlayer capacity and ensure efficient high-frequency isolation, it is necessary that the power and ground layers are adjacent. Power supply sites should be located in the inner layers of the multilayer printed circuit board. The power supply layers

should be made as continuous as possible, reducing the area of non-metallized areas;

- place all high-frequency circuits in the inner layers adjacent to the GND layers. Changing the direction of the route of the conductor of high-speed signals in the topology of the multilayer printed circuit board to perform in the form of an arc;
- the entire space of the printed circuit board, which does not house the components of the circuit and the communication line, must be filled with a landfill;
- separate power supply buses of digital and analog circuits;
- I/O wires of the printed circuit board should be made as short as possible and provide for filtering of output signals.

Results

To reduce the interference of the product, various circuit solutions are used (primarily radio interference filters), designed to suppress the spectral components of the fundamental frequencies at which the product operates and their harmonics; specialized materials and coatings (silver, brass, etc.) are used, which reduce the level of EMF emitted; structural elements of grounding of a product and elements of metallization of its parts are used.

To evaluate the effectiveness of circuit and design solutions, which are the basis for the design of a product of avionics class BCOM (on-board digital computer), a series of experiments was conducted. The level of EMF emitted by the product in the frequency range 0.01 MHz - 100 MHz was subject to evaluation.

The results of the experiments are shown in Fig. 4.8.

Separately in fig. Figure 1a shows a graph of the level of EPM recorded during operation of the product in the frequency range 0.01 MHz - 30 MHz, in Fig. 7 b - in the frequency range of 30 MHz - 100 MHz. Different lines on the graphs show the level of registered EMF and the allowable level that meets the requirements of regulatory and technical documentation for this class of equipment.

The presence of pronounced EMF pulsations in the low-frequency region is explained by the peculiarities of the product and is associated with the clock frequency of information exchange of goods with other subscribers of the bots of the complex through communication channels.

In the high frequency region, the level of allowable EMF is constant, and the pulsations of the EMF emitted by the product are due to the operation of the product at the clock frequency of the processor used in the product, with additional EMF generation at fundamental frequencies. It is important to note that harmonics occur both at the main frequency of the product and at the combined frequencies generated by the operation of the product nodes (input devices, intermodule bus, etc.) at frequencies other than the main.

Discussion

In the course of the research the existing types of test control of onboard digital computer systems were analyzed. To date, in most practical applications, the computer system is tested in the background on a parallel test scheme by internal control of structural and functional modules and on a sequential test scheme at the factory. However, this method of control does not meet the requirements for advanced types of computers in accordance with the concept of integrated modular avionics. The used test scheme when detecting the failure of one module generates a failure signal of the entire computer system, which eliminates the possibility of reconfiguration of the aircraft complex at the intrasystem level.

Conclusions

1. The analysis of existing methods and algorithms of control and diagnostics of computer systems of the perspective aircraft is carried out. it is shown that for the computer systems of the 4th generation the consistent principle of construction of testing was used. It is proposed to use the parallel principle of testing for advanced computer systems.

2. The physical scheme of connections of a local area network within a computer system that allows to implement various logical connections proceeding from the necessary

functional task is constructed. Variants of logical connections affect reliability indicators. A backup scheme at the level of identical modules is preferred.

3. The unification of the verification workplace, which is used to configure and verify the components of the computer system of a promising aircraft, is proposed. it is shown that for the whole nomenclature of computer modules of the IMA class it is possible to use the unified workplace of check with application of necessary technological modules of check.

4. Experiments to assess the temporal characteristics of the tests and functional software on a real product. It is shown that the structure of the product affects the temporal characteristics of the cycle of the onboard task.

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EXPERIMENT TEST OF THE RELIABILITY OF COMPUTER SYSTEMS OF INTEGRATED MODULAR AVIONICS

The tasks of designing advanced computer systems in the class of integrated modular avionics (IMA) structures are relevant. The development of IMA computing modules requires the development of inspection schemes and software specialized for IMA class products, both in the process of operation on the aircraft and in the production process at the factory. Unification of IMA modules will allow to build the automated workplace on checking of products that possesses the raised indicators of unification and standardization of design solutions. Objective is to assess the reliability of computer structures of integrated modular avionics for different configurations of hardware. The obtained results are based on the use of methods of systems theory, methods of mathematical modeling, methods of reliability theory, methods of probability theory. Reliability assessment is performed by analytical derivation of the expression for the probability P(t) of trouble-free operation of the product. And also the unified topology of the internal network of the calculator on the basis of space wire exchange channels and variants of its execution for various onboard applications is offered. Equivalent reliability schemes of each of the personal structures are presented and the probabilities of trouble-free operation of each structure are analyzed. A series of experiments was conducted to evaluate the effectiveness of circuit and design-technological solutions, which are the basis for the design of avionics products of the class of on-board digital computer. The level of the radiated electromagnetic interference in the frequency range 0.01 mhz - 100 mhz was evaluated. The physical scheme of connections of a local area network is offered. Inside the computer system allows to realize Various logical connections proceeding from the necessary functional task. Variants of logical connections affect reliability indicators. The scheme of Reservation at the Level of Identical modules is better. An experiment was performed to evaluate the Temporary performance characteristics of tests and functional software on a real product. It is shown that the structure of the product affects the Temporary characteristics of the cycle Execution of the onboard task. An algorithm for controlling a computer system during a flight is proposed. It is established that for perspective computer systems it is necessary to use "External" initiated testing with introduction of memorization of results of testing of functional components. A series

of experiments on testing modules using the proposed algorithms. Temporary characteristics of the product testing algorithm are shown. Reliability assessment was performed for three cases of organization of the internal structure of the computer system of the IMA class.

***Keywords**: integrated modular avionics, computing systems, assessment of reliability indicators, probability of failure-free operation.*

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ЕКСПЕРИМЕНТАЛЬНА ОЦІНКА НАДІЙНОСТІ КОМП'ЮТЕРНИХ СИСТЕМ ІНТЕГРОВАНОЇ МОДУЛЬНОЇ АВІОНІКИ

Актуальною є задача проектування перспективних обчислювальних систем в класі структур інтегрованої модульної авіоніки (IMA). Для розробки обчислювальних модулів IMA потрібна розробка схем перевірок і програмного забезпечення, спеціалізованих під вироби класу IMA, як в процесі експлуатації на повітряному судні, так і в процесі виробництва на заводі-виробнику. Уніфікація модулів IMA дозволить побудувати автоматизоване робоче місце по перевірки виробів, що володіє підвищеними показниками уніфікації та стандартизації проектних рішень. Метою роботи є оцінки надійності обчислювальних структур інтегрованої модульної авіоніки для різних конфігурацій апаратних засобів. Отримані результати, засновані на використанні методів теорії систем, методів математичного моделювання, методів теорії надійності, методів теорії ймовірностей. Оцінка надійності проводиться шляхом аналітичного виведення виразу для ймовірності P(t) безвідмовної роботи виробу. А також пропонується уніфікована топологія внутрішньої мережі обчислювача на базі каналів обміну SpaceWire і варіанти її виконання для різних бортових додатків. Представлені еквівалентні схеми надійності кожної з особистих структур і аналізуються ймовірності безвідмовної роботи кожної структури. Для оцінки ефективності схемних і конструктивно-технологічних рішень, покладених в основу проектування виробу авіоніки класу бортової цифрової обчислювальної машини, була проведена серія експериментів. Оцінці підлягав рівень випромінюваних виробом електромагнітної перешкоди в діапазоні частот 0,01 МГц – 100 МГц. Результати. Запропонована фізична схема з'єднань локальної мережі всередині обчислювальної сис-теми, що дозволяє реалізовувати різні логічні з'єднання, виходячи з необхідного функціонального завдання. Варіанти логічних з'єднань впливають на показники надійності. Кращою є схема резервування на рівні ідентичних модулів. Проведено експерименти з оцінки тимчасових характеристик роботи тестів і функціонального програмного забезпечення на реальному виробі. Показано, що структура виробу впливає на тимчасові характеристики циклу виконання бортового завдання. Запропоновано алгоритм контролю обчислювальної системи під час польоту. Встановлено, що для перспективних обчислювальних систем слід використовувати «зовнішнє» ініційоване тестування з введенням мажорування результатів тестування функціональних компонентів. Проведена серія експериментів з тестування модулів з використанням запропонованих алгоритмів. Показані тимчасові характеристики роботи алгоритму тестування вироби. Проведено оцінку надійності для трьох випадків організації внутрішньої структури обчислювальної системи класу IMA.

***Ключові слова**: інтегрована модульна авіоніка, обчислювальні системи, оцінка показників надійності, ймовірність безвідмовної роботи*