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ABOUT THE PHASE NOISE OF FREQUENCY SYNTHESIZERS

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***Abstract*—*The paper proposes a variant of implementing a partial synthesizer with a small frequency step and preserving a sufficient level of phase noise in the X-band frequency range, which provides high frequency stability and low phase noise by combining 3 methods. A brief review of common methods for constructing frequency synthesizers, such as phase-locked loop, digital signal synthesis (DDS), dielectric resonator oscillator, is given. Their advantages and disadvantages were used and taken into account in the development of a new method for constructing a frequency synthesizer. The article compares the characteristics of the phase-locked loop frequency synthesizer on the ADF5355 chip with the developed method. The proposed method, which includes all 3 proposed methods, is presented in the form of a functional circuit containing two phase-locked loops and one DDS. The first PLL contains a dielectric resonator oscillator with an output signal of 8 GHz and a working frequency bandwidth of 1 kHz with a minimum phase noise equal to –132.85 dBc/Hz at a 1 kHz offset. The low-noise DDS signal is fed to the second phase-locked loop. The output signal is in the range of 9-9.5 GHz with a phase noise of –98.32 dBc/Hz at a 10 kHz offset.*

Keywords—Dielectric resonator oscillator; digital signal synthesis; frequency range; frequency synthesizer; functional circuit; phase noise; phase-locked loop.

I. INTRODUCTION

Almost all receiving and transmitting devices of various types and purposes use frequency synthesizers. Two commonly used methods of building synthesizers are phase-locked loop (PLL) and digital signal synthesis (DDS). The article discusses some aspects of these methods. The advantages of PLL synthesizers are their relative simplicity of construction and versatility of use. The general functional diagram (Fig. 1) contains a reference oscillator, a phase detector and a low-pass filter.

A linearized differential equation for the phase difference Φ_Δ PFD input signals at condition of $\Phi_\Delta 90^\circ$

$$\frac{d\Phi_\Delta}{dt} = \omega_\Delta - K\Phi_\Delta, \quad (1)$$

difference in frequencies coming to the PDF. K is the contour factor.

Solution of (1)

$$\Phi_\Delta(t) = e^{-Kt}\left(\Phi_{\Delta 0} - \frac{\omega_\Delta}{K}\right) + \frac{\omega_\Delta}{k}, \quad (2)$$

where $\Phi_{\Delta 0}$ is the initial phase angle.

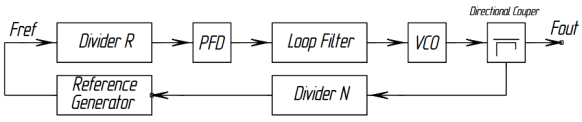

Fig. 1. Functional diagram of the PLL frequency synthesizer

The phase noise level is one of the main parameters in frequency synthesizers. Physically, it is the difference in power between the lowest signal and the signal above 1 Hz. The phase noise level is one of the main parameters in frequency synthesizers. Physically, it is the difference in power between the lowest signal and the signal above 1 Hz. There are various ways to improve this parameter: frequency multiplication instead of division, better reference signal parameters, a different element base [2], [3].

II. PROBLEM STATEMENT

The negative effect of phase noise contributes to the appearance of sidebands and harmonics that degrade the frequency synthesizer spectrum, and the ability to distinguish the carrier signal from the noise signal is reduced. In communication systems, this causes the reflected signal to be masked from the target, making it difficult to detect it and obtain accurate data on the target's speed and range [4] – [6].

The frequency division ratio N increases as the tuning step decreases. Therefore, by using a low-pass filter and combinations of digital and analog circuits, the N factor can be reduced.

Phase-locked loop frequency synthesizers exist with both fractional and integer division of N.

The integer method is simple, while the fractional method gives high speed of analog and digital PLLs.

A phase-locked loop frequency synthesizer refers to an indirect DDS [7], [8]. There are also direct digital frequency synthesizers that consist of a digital-to-analog converter (DAC), a phase accumulator, and a phase amplitude converter (Fig. 2).

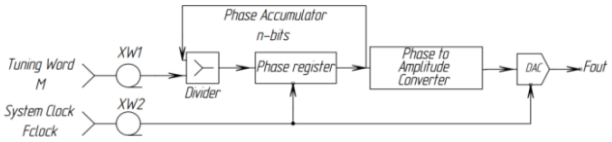

Fig. 2. The DDS synthesizer structure

Digital signal synthesis are currently developing rapidly and improving their performance. But despite this, the highest frequency value of DDSs, for example, from Analog Devices reaches only 12.3 GHz [9], which does not allow them to be used in the X frequency band.

Therefore, the aim of the work is to use known methods of building frequency synthesizers and develop an improved frequency synthesizer on their basis.

Having studied the method of building a PLL on the example of the ADF5355 chip from Analog Devices [10], the results were as follows. According to the data sheet, the phase noise value at a 100 kHz offset from the 10 GHz carrier signal is –107 dBc/Hz. After modeling in the ADlSimPLL software environment, the results are shown in (Fig. 3).

The results of empirical studies of the phase noise of the ADF5355 are shown in Fig. 4.

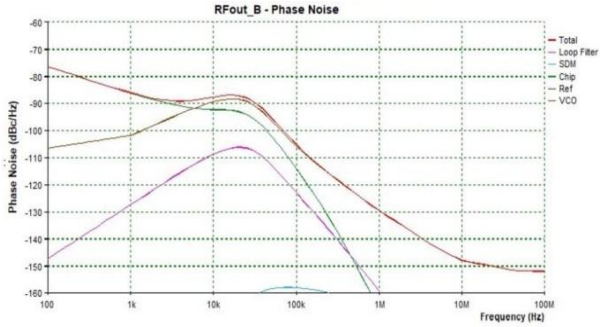

Fig. 3. Phase noise of the PLL on the basis of ADF5355 on frequency 10 GHz due to the results of mathematical modeling in ADlsimPLL

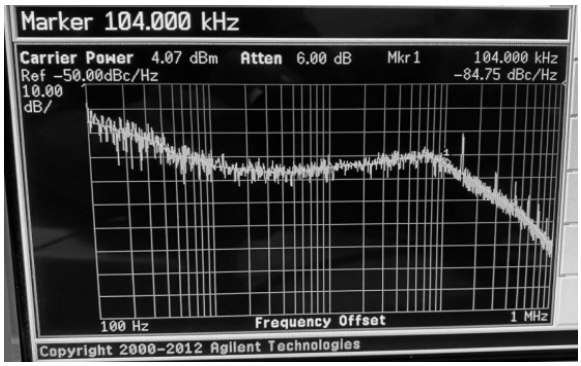

Fig. 4. The experimental study of the phase noise PLL with ADF5355

III. PROBLEM SOLUTION

A component of phase noise is a quartz oscillator, which contributes to its deterioration. You can calculate phase noise using the following formulas [2].

$$N_{\text{out\_ref}} = \frac{0/5N_{\text{ref}}}{f/f_{\text{ref}}} \cdot \frac{G_{\text{loop}}(f)}{R}, \qquad (3)$$

where, N_{ref} phase noise of the reference oscilator (crystal oscillator), the closed; G_{loop} gain, R frequency division factor of the reference frequency.

A phase detector also contributes to the phase noise of the output signal.

$$N_{\text{out\_pd}} = 10^{0.05\left(N_{\text{pd\_ref}} + 10\log f_{\text{ref}}\right)} \cdot G_{\text{loop}}(f), \qquad (4)$$

where, $N_{\text{pd\_ref}}$ phase noise value of the phase detector. Another major source of phase noise is the voltage-controlled oscillator (VCO), whose value depends on the frequency.

$$N_{\text{VCO}}(f) = \frac{0.5N_{\text{VCO\_ref}}}{f/f_{\text{vco\_ref}}} \cdot \frac{1}{1+G_{0\_\text{loop}(f)}}, \qquad (5)$$

where, $f_{\text{VCO}}(f)$VCO operating frequency; $G_{0\_\text{loop}(f)}$ is the open-loop gain.

Based on the work of Leeson [11], it is proved that the oscillator circuit with high quality has lower values of phase noise. And the best resonators with high Q are DROs with Q values of 50–70 k and a phase noise level at a 1 kHz shift of –165 dBc/Hz.

Also, low phase noise levels are reported in other works [12], but the peculiarity is that such values can be achieved only at the resonant frequency.

There are also YIR generators that are better in terms of performance compared to DROs, but such performance is achieved by increasing the

complexity of the structure, weight, and overall dimensions.

To confirm the low phase noise level of the DRO, we took the PLDRO-10-7000-5P at 7 GHz to be an example and programmed a mathematical model in the ADlsimPLL software environment (Fig. 5).

Dielectric resonant oscillators operate at a tuned resonant frequency and have a narrow bandwidth close to 1 kHz, which minimizes phase noise.

Based on the results of the study, the following structural diagram of the frequency synthesizer (Fig. 6) was developed and proposed.

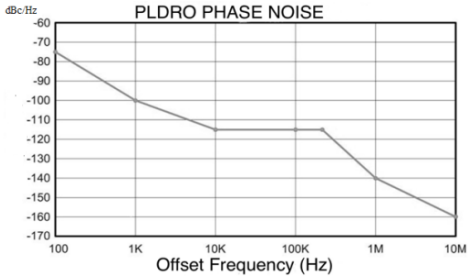

Fig. 5. Simulation results of PLDRO-10-7000-5P phase noise

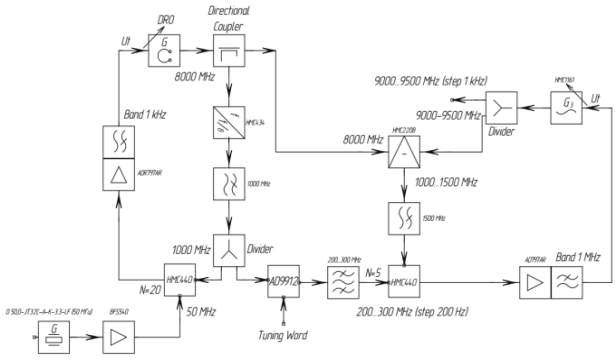

Fig. 6. The functional diagram of the *X* band frequency synthesizer

The block diagram is being drawn up:

- DDS;
- two PLLs;
- phase detector (HMC440);
- low-pass filter of 1 kHz on a low-noise operational amplifier ADR797AR;
- DR;
- phase shifter;
- HMC434 divider by 8;
- low-pass filter for 1000 MHz;
- splitter.

Phase-Locked Dielectric Resonator Oscillator (PLDRO), which is configured for 8 GHz, has an output signal with a low phase noise level equal to – 133 dBc/Hz at a 1 kHz offset from the carrier signal, and close to the *X* band. This, in turn, makes it possible to avoid significant frequency division factors that affect the increase in the phase noise of the output signal of the frequency synthesizer

But since the PLDRO bandwidth is narrow, around 1 kHz, for this reason, the AD9912 DDS generator with a 14-bit DAC is used. It provides a tuning step in the operating range of the frequency synthesizer and a low-noise signal, with a step of 200 Hz.

A low-pass filter consists of two filters, a low-pass filter and a high-pass filter, to produce the required bandwidth (Fig. 7).

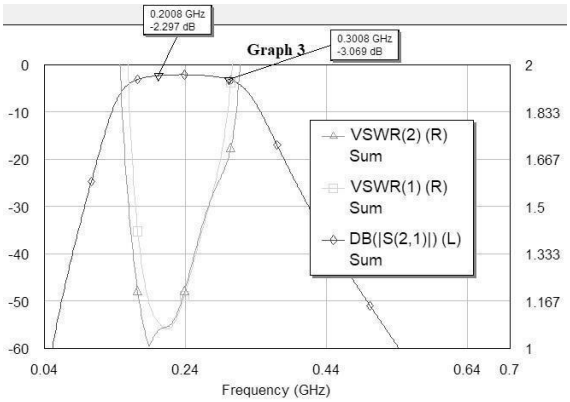

Fig. 7. Frequency responses of passband filter. Left axis shows filter attenuation in dB and right axis – standing wave ratio by voltage (VSWR)

HMC2208BMS which is used in the second PLL as a dual balanced mixer. It outputs a 9 ... 9.5 GHz VCO oscillation to the HMC1161. A low-pass filter removes the 1...1.5 GHz spurs and feeds them to a divider with a division factor of $N = 5$, which also serves as a phase detector for the second loop. The last part of the second circuit is a low-pass filter operating at 1 MHz and an AD898AR power suppressor. The frequency response of the low-pass filter is shown in (Fig. 8).

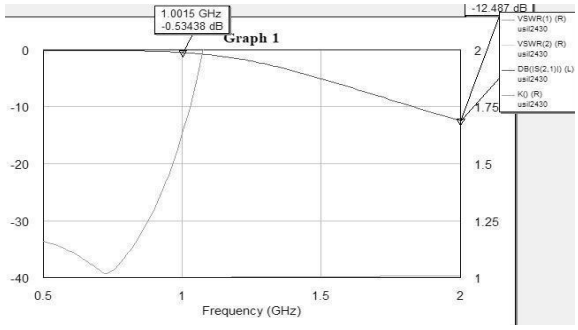

Fig. 8. Frequency responses of attenuation and VSWR LPF

As a result of the implementation of the prototype of the microwave frequency synthesizer according to the functional diagram (see Fig. 6), it was possible to achieve a phase noise level of – 101.89 dBc/Hz at a

100 kHz offset (Fig. 9), which is much better than the first version on the ADF5355 chip.

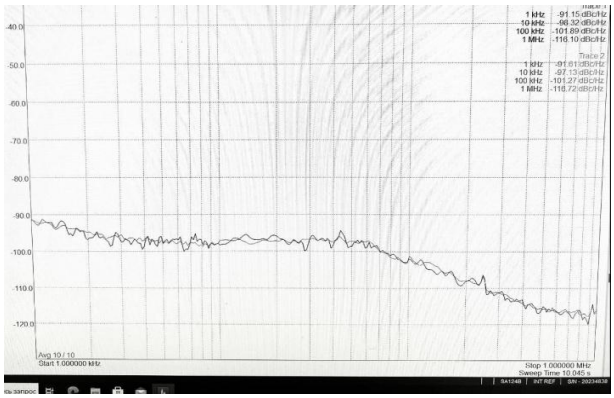

Fig. 9. Phase noise response of frequency oscillator on 9 GHz

IV. CONCLUSIONS

As a result of the research and development of the microwave frequency synthesizer, all known and existing methods of construction were realized, a new method was implemented that covered the advantages of other methods and combined them in one. The new method of construction uses PLDRPO which has a bandwidth of 1 kHz and a tuning bandwidth of 10 MHz with an output frequency of 8 GHz. An important advantage and reason for using the PLDRO as a reference oscillator is its 8 GHz output signal, which is stable and with low phase noise, which is used in the second stage. With the help of DDS in the frequency synthesizer, the second component, namely the tuning step, can be achieved.

The digital signal synthesis bandwidth is 200...300 MHz and the tuning step is 200 Hz, and its output signal also provides a low level of phase noise.

REFERENCES

[1] Venceslav F. Kroupa, Phase Lock Loops and Frequency Synthesis. John Wiley Ltd., 2003. ISBN 0-470-84866. https://doi.org/10.1002/0470014105

[2] Lance Lascari, "Phase Noise Prediction in PLL Synthesizers," *Applied Microwave & Wireless*, 12, 4 April (2000). Corpus ID:17800386

[3] Xinyu Zhang, Qifei Du, Cheng Liu, Yue Ma, Yefei Li, and Jinhuan Li, "A Low Phase Noise Frequency Synthesizer with a Fourth-Order RLC," *Electronics*, 12, 224, 2023. https://doi.org/10.3390/electronics12010224

[4] Amin Walter Doerry, "Radar Receiver Oscillator Phase Noise," *Sandia National Laboratories*, SAND2018-3614, (2018)

[5] Gao Hiang, Klumperink Eric, Nauta Bram.: Sub-Sampling PLL Technology, Jan. (2020), doi: 10.1049/PBCS064E-ch21

[6] Eric Loria, Samuel Prager, Ilgin Seker, Razi Axmed, Brain Hawkins, and Mario Lavalle, "Modelling the Effects of Oscillator Phase Noise and Synchronization on Multistatic SAR Tomography," *IEEE Trans. on Geoscience and Remote Sensing*, 61 2023. https://doi: 10.1109/TGRS.2023.3249637

[7] Tong Leri and Lia Liang, "Research and Design of Digital Unit for Direct Frequency Synthesizer. Journal of Physics," *Conference Series*, 1907, 2021. https://doi: 10.1088/JSSC.2015.2468712

[8] Stefan Leitner, Haibo Wang, Tragoudas Spyros.: Design Techniques for Direct Digital Synthesis Circuits with Improved Accuracy over Wide Frequency Ranges. Journal of Circuits, Systems and Computers, 26, 2, 2017. https://doi:10.1142/S0218126617500359

[9] Direct Digital Synthesis. Analog Devices, Inc., 2024. https://www.analog.com/en/parametricsearch/11018#/

[10] Microwave Wideband Synthesizer with Integrated VCO ADF5355. Analog Devices, 2017.

[11] D. B. Leeson, "A simple model of feedback oscillator noise spectrum," *Proceedings of the IEEE*, vol. 54, 2 1966. https://doi:10.1109/PROC.1966.4682

[12] Liang Zhou, Wen Yan Yin, Jiang Wang, and Lin-Sheng Wu, "Dielectric Resonators With High Q-Factor for Tunable Low Phase Noise Oscillators," *EEE Trans. on Components, Packaging and Manufacturing Technology*, vol. 3, no. 6, JUNE 2013. https://doi: 10.1109/TCPMT.2013.2258465

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Я. В. Грицев. Про фазовий шум синтезаторів частоти
У статті запропоновано варіант реалізації часткового синтезатора з малим кроком зміни частоти та збереженням достатнього рівня фазового шуму в X-діапазоні частот. Наведено короткий огляд поширених методів побудови синтезаторів частоти, таких як петля фазового автопідстроювання частоти, генератор прямого цифрового синтезу, діелектричний резонаторний генератор. Запропонований метод представлений у вигляді функціональної схеми, що містить дві петлі фазового автопідстроювання частоти і один генератор прямого цифрового синтезу. Перша петля фазового автопідстроювання частоти містить діелектричний резонаторний генератор з вихідним сигналом 8 ГГц, з фазовим шумом – 132,85 дБс/Гц при зсуві 1 кГц. Сигнал DDS з низьким рівнем шуму подається на другий фільтр низьких частот. Вихідний сигнал знаходиться в діапазоні 9–9,5 ГГц з фазовим шумом – 98,32 дБс/Гц при зсуві 10 кГц. Результати дослідження були використані для радіолокаційної станції завад, та успішно виконують свою функцію.
Ключові слова: фазовий шум; синтезатор частот; частотний діапазон; функціональна схема; фазоамплітудна підстройка частоти; цифровий синтезатор частоти; генератор на діалектричному резонаторі.

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