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AUTOMATED TECHNOLOGICAL DESIGN OF NANOSCALE TRANSISTORS

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Abstract*—The article is devoted to the automation of technological preparation of modern high-frequency and energy-efficient bipolar transistors with nanoscale depths of impurity implantation into a nanoconductor substrate. At the stage of mathematical modeling of technological operations of multilayer casting, the known theoretical and empirical, developed by the authors of the article, high-temperature dependences of doping parameters, distributions of depths of boundary distances of emitter and collector junctions, which, as a result, determine the thickness of the electrically neutral base region of the transistor, are taken into account. Mathematical models of technological parameters of surface and volume concentrations of impurities, which cause degeneration and repeated inversion of the conductivity types of the initial crystalline substrate, are proposed. The maximum possible values of the tincture and solution of acceptor and donor impurities, which increase the gain coefficients and reduce the power consumption of bipolar nanotransistors, are determined. The drift components of the base and collector currents, which are caused by the internal electric field of the inhomogeneous base, are taken into account. The temperature and time dependences of technological doping operations are found, which primarily determine the creation of bipolar transistors with a base thickness from 100 nm to 10 nm. The values of the limiting concentrations of impurities in semiconductor structures are established. Examples are considered that confirm the effectiveness of the proposed methods for automated design of bipolar nanotransistors. In the future, it is planned to develop generalized algorithms for multi-level hierarchical modeling of transistor nanoelectronics components.*

Keywords—Automation of technological preparation; transistor nanoelectronics; impurity implantation; electron-hole junction; electroneutral base; gain.

I. INTRODUCTION

Modern incentives for the development of microelectronics require a reduction in the size of semiconductor devices, in particular bipolar transistors, which allows to increase their speed, reduce power consumption and increase the functional density of integrated circuits [1]. With a decrease in the geometric dimensions of active elements, the influence of technological factors on their electrical characteristics increases critically. One of the key aspects of design is the accurate modeling of diffusion doping processes, which determine the position of electron-hole transitions and the width of the basic electroneutral region. The formation of a proper impurity profile in nanometer scale conditions requires the use of mathematical models to optimize technological modes [2].

II. THE PURPOSE OF THE WORK AND THE STATEMENT OF THE PROBLEM

The purpose of the study is to numerically simulate the process of two-stage diffusion of acceptor and donor impurities in a silicon semiconductor for the formation of emitter and collector junctions of a bipolar nanotransistor. The task of the study is to build a one-dimensional model of the distribution of concentrations of acceptor and donor impurities taking into account the temperature dependence of the diffusion coefficients, the solubility limit, the time and sequence of thermal treatment. It is necessary to determine the depth of the junctions, the width of the base and to assess the influence of the technological modes of the drive and acceleration on the formation of doped regions. The calculation of the current gain in a circuit with a common emitter for typical geometric scales of nanostructures is also implemented.

III. MATHEMATICAL MODEL

In forming the structure of a bipolar transistor, it is necessary to create two junctions. The scheme of a discrete vertical bipolar transistor formed using standard planar technology is shown in Fig. 1. Such a transistor can be formed, for example, if an

acceptor impurity is first introduced into *n*-type silicon, and then a donor impurity [2].

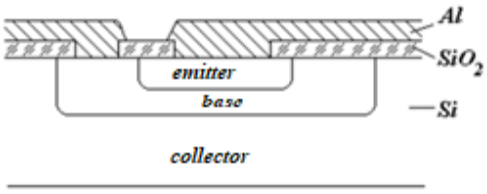


Fig. 1. Structure of the technological modeling for a planar transistor

Since donor and acceptor impurity atoms diffuse into the semiconductor at different rates, it is possible to create the appropriate surface concentration of these elements and obtain an electron-hole structure by simultaneous diffusion of both elements from the vapor phase. To obtain diffusion transitions in silicon, along with the method of simultaneous diffusion of impurities, for example, from compounds of groups III–V, the method of sequential diffusion of acceptor and donor impurities or their alloys, or compounds, especially oxides, is used.

The first method, although simple, does not allow separate control of the impurity concentration or temperature. Therefore, the second method, which allows separate control of the concentration and temperature, is usually preferred. First, a slowly diffusing impurity (donor) is introduced into the semiconductor, otherwise it will be difficult to control the distribution of the faster diffusing impurity (acceptor).

For better control of the process, it is necessary that both impurity elements are present in the semiconductor only during the second diffusion. In the case when the concentrations can be set independently of the temperature, carrying out both diffusion cycles at different temperatures provides greater flexibility of the technological process. Even when the diffusion coefficients of the donor and acceptor are the same, the process can be controlled by varying the duration of the first and second cycles.

The basic diffusion is usually carried out in two stages: the drive and the acceleration. The drive stage is carried out for a short time and in this case the amount of impurity is strictly regulated.

The impurity concentration distributions and the temperature dependence of the diffusion coefficient are given according to the diffusion process model [3]. The impurity concentration distribution is described by the additional Gaussian error *erfc* – function:

$$C_1(x) = C_0 erfc \frac{x}{2\sqrt{D_1 t_1}}. \quad (1)$$

The surface concentration of acceptor impurities is calculated using the model [3]:

$$Q = C_0 \cdot \sqrt{\pi D_1 t_1}, \quad (2)$$

where Q is the surface concentration of the acceptor impurity; C_0 is the surface concentration of the impurity during the confinement process; D_1 is the intrinsic diffusion coefficient of the impurity during confinement; t_1 is the diffusion time of acceptors during confinement, which is subject to exponential distributions.

The second stage is carried out for a longer time, and the distribution of the donor impurity:

$$C_2(x) = \frac{Q}{\sqrt{\pi D_2 t_2}} \exp\left(-\frac{x^2}{4 D_2 t_2}\right), \quad (3)$$

where D_2 is the intrinsic diffusion coefficient of donors during the acceleration process; t_2 is the acceleration time of the impurity.

The depth of the transition is determined by the exponential distribution method of the impurity given in [4]:

$$X_i = 2\sqrt{D_2 t_2} \sqrt{\ln\left(\frac{Q}{C_s}\sqrt{\pi D_2 t_2}\right)}, \quad (4)$$

where C_s is the concentration of the donor impurity in the substrate of the original semiconductor.

The diffusion of the emitter region is carried out in one stage, usually from a source with a constant surface concentration, therefore the distribution of donors is also described by the *erfc*-function:

$$C_3(x) = C_0 \cdot erfc \frac{x}{2\sqrt{D_3 \cdot t_3}}, \quad (5)$$

where D_3 is the intrinsic diffusion coefficient of the emitter impurity; t_3 is the diffusion time of the emitter impurity.

The depth of the emitter junction is determined by the inversion threshold of the substrate conductivity type. To calculate the depth of the junction, it is necessary to solve the first-order kinetic equation:

$$C_3(x) + C_S = C_2(x). \quad (6)$$

The exact calculation of the depth of the transition in analytical form is very complex [5], therefore equation (6) is solved numerically.

The temperature dependence of the diffusion coefficient has the form:

$$D = D_0 \exp\left(-\frac{\Delta E}{kT}\right), \quad (7)$$

where D_0 is the diffusion coefficient at infinitely high temperature, cm^2s^{-1}, E is the diffusion activation energy, eV, $k = 8.625 \cdot 10^{-5}$ eV/K is the Boltzmann constant.

The calculation of the static base current gain in a common-emitter circuit is performed taking into account the emitter efficiency and transfer coefficient and corresponds to the classical model given in [6]:

$$\gamma = \frac{\partial A J_p(x=0)}{\partial I_E} = \left[1 + \frac{n_E}{p_B}\frac{D_E}{D_B}\frac{L_B}{L_E}\text{th}\left(\frac{W}{L_B}\right)^{-1}\right], \quad (8)$$

$$\alpha_T = \frac{J_p(x=W)}{J_p(x=0)} = \frac{1}{\text{ch}\left(\frac{W}{L_B}\right)} \approx 1 - \frac{W^2}{2L_B^2}, \quad (9)$$

where L_B is the diffusion length of holes in the base; L_E is the diffusion length of electrons in the emitter; A is the cross-sectional area of the transistor; p_B is the equilibrium density of minority carriers in the base.

Note that $\gamma < 1$ and $\alpha_T < 1$, and the quantities that complement them to, are proportional to the electronic component of the base contact current. In an idealized bipolar transistor with a base width less than $0.1\,L_B$, $\alpha_T > 0.995$, therefore, the current gain is almost completely determined by the emitter efficiency, provided that $\alpha_T \approx 1$:

$$\beta = \frac{\gamma}{1-\gamma} = \frac{p_B D_B I_E}{L_E D_E L_B}\text{cth}\left(\frac{W}{L_B}\right). \quad (10)$$

IV. Modeling in MathCad

We set constants and formulas in MathCad to model the diffusion process of a nanoscale transistor (Table I).

TABLE I. Parameters of Technological Stage

Parameters	Arsenic, As	Boron, B	Technologist conditions
Diffusion coefficient, D_0, cm^2s^{-1}	24	5.1	Arsenics driving T_1=1273ºC, t_1 = 900 s Arsenics dispersion T_2=1373ºC, t_2 = 3600 s Borons diffusion T_3=1273ºC, t_3 = 300 s Donors concentration in the silicon substrate $Nc = 10^{17}$ cm^3
Activation energy, Ea, eV	4.08	3.7	
Surface concentration, N_0, cm^3	$3 \cdot 10^{19}$	10^{21}	
Maximum solubility in silicon substrate, M, cm^3	$2 \cdot 10^{21}$	$4 \cdot 10^{20}$	

We set equations in MathCad to calculate the technological stage:

a) calculation of distribution for the atoms boron B introduced during the first stage (driving):

$$D(T) := DoB \cdot \exp\left(-\frac{EaB}{k \cdot T}\right)$$

$$N1(x) := \begin{cases} No_1 \cdot \left(1 - \text{erf}\left(\frac{x}{2 \cdot \sqrt{D(T_1) \cdot t_1}}\right)\right) & \text{if } No_1 < MB \\ MB \cdot \left(1 - \text{erf}\left(\frac{x}{2 \cdot \sqrt{D(T_1) \cdot t_1}}\right)\right) & \text{otherwise} \end{cases}$$

b) calculation of distribution for the atoms boron B introduced during the second stage (dispersion):

$$Q := Nc \cdot \sqrt{\pi \cdot D(T_2) \cdot (t_2 \cdot t_3)}$$

$$N2(x) := \frac{Q}{\sqrt{\pi \cdot D(T_2) \cdot (t_2 + t_3)}} \cdot \exp\left[-\frac{x^2}{4 \cdot [D(T_2) \cdot (t_2 + t_3)]}\right]$$

$$D(T_2) = 1.375 \times 10^{-13}$$

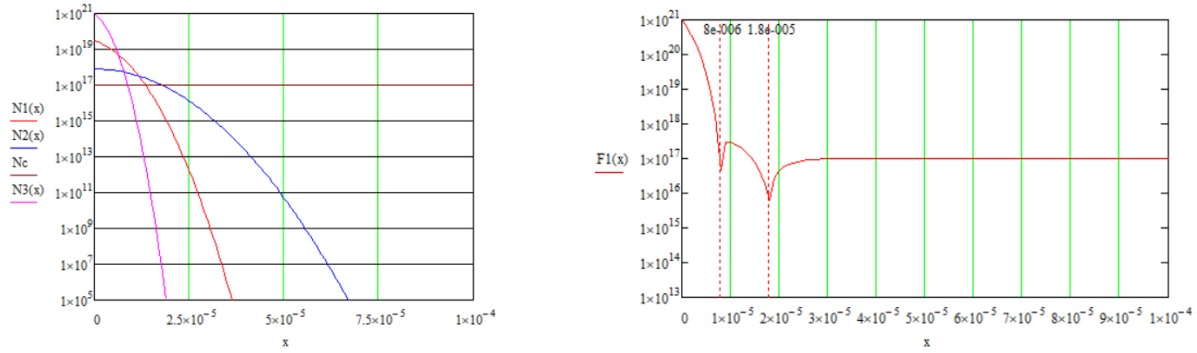
c) calculation of distribution for the atoms arsenic As introduce during the third stage (diffusion):

$$DAs(T) := DoAs \cdot \exp\left(-\frac{EaAs}{k \cdot T}\right)$$

$$D3 := DAs(T_3) \qquad D3 = 2.614 \times 10^{-14}$$

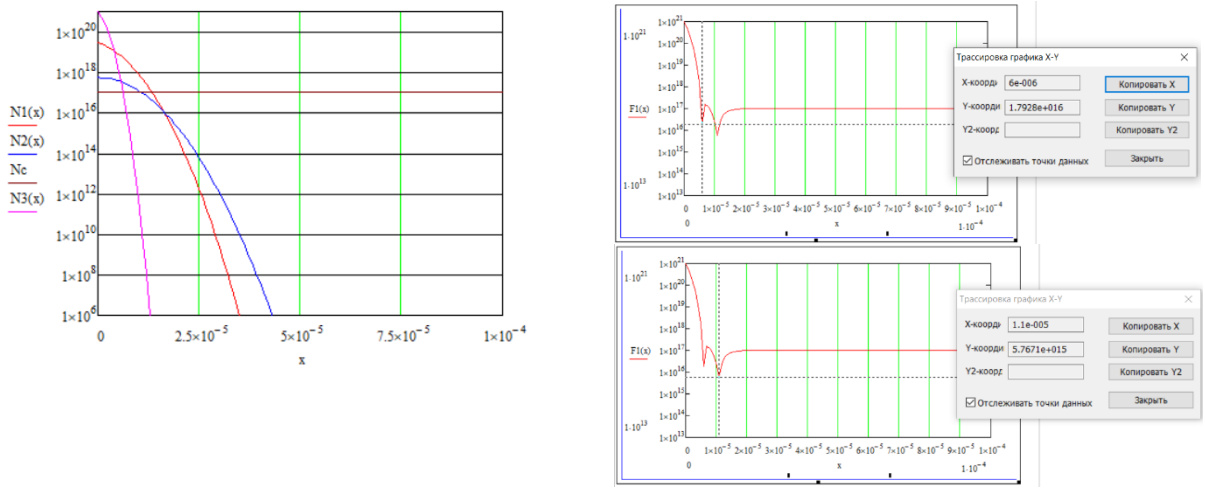
$$N3(x) := \begin{cases} No_3 \cdot \left(1 - \text{erf}\left(\frac{x}{2 \cdot \sqrt{DAs(T_3) \cdot t_3}}\right)\right) & \text{if } No_3 < MAs \\ MAs \cdot \left(1 - \text{erf}\left(\frac{x}{2 \cdot \sqrt{DAs(T_3) \cdot t_3}}\right)\right) & \text{otherwise} \end{cases}$$

After simulating in the MathCad environment, concentration distributions (Figs 2, 3 and 4) of impurities in the wafer substrate were obtained for different stages of diffusion and the depth of the emitter and collector junctions of nano-sized transistors with an electroneutral base width of 100, 50, 20 nm.



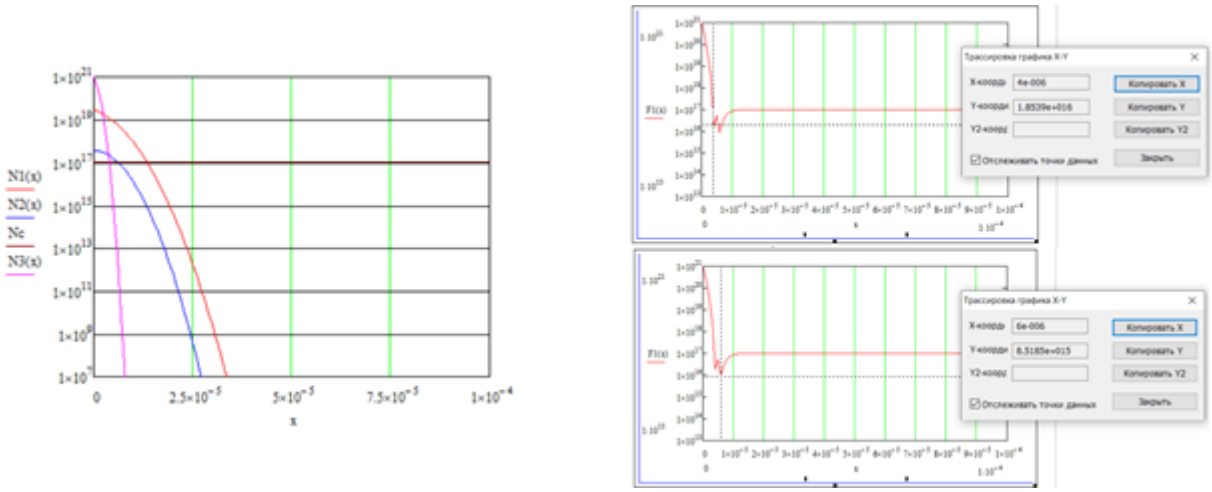
a) b)

Fig. 2. Results of simulating in the MathCad environment for a nanotransistor with a base width of 100 nm, when and: (a) is the distribution of impurity concentration over the depth of the substrate for different stages of diffusion; (b) is the depths of the emitter and collector junctions



a) b)

Fig. 3. Results of simulating in the MathCad environment for a nanotransistor with a base width of 50 nm, when and: (a) is the distribution of impurity concentration over the depth of the substrate for different stages of diffusion; (b) are depths of the emitter and collector junctions

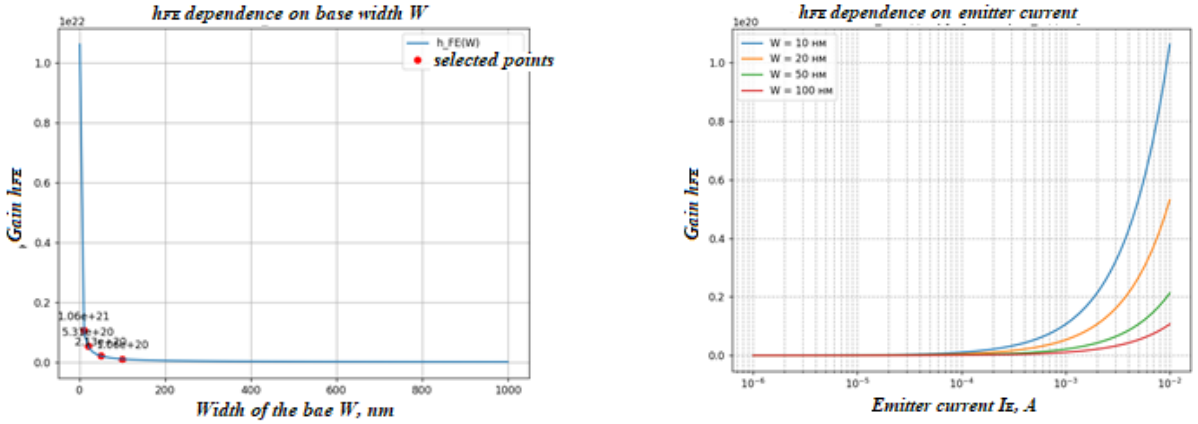


a) b)

Fig. 4. Results of simulating in the MathCad environment for a nanotransistor with a base width of 20 nm, when and: (a) is the distribution of impurity concentration over the depth of the substrate for different stages of diffusion; (b) is the depths of the emitter and collector junctions

Using equation (10), the dependences of the static current gain coefficient β on the thickness of the electroneutral base W from 1 μm to 1 nm were calculated, when the initial modeling parameters were: $p_B = 1\times10^{13}$ cm^3, $L_B = 104$ cm, $L_E = 2\times10^4$ cm, $D_E = 24$ cm^{2}s^{-1}, $D_B = 5.1$ cm^{2}s^{-1}, $I_E = 1$ mA.

The graphs of the dependences of the current gain coefficient β in a circuit with a common emitter on the thickness of the electroneutral base and on the emitter current are shown in Fig. 5a and b, respectively.



a) b)

Fig. 5. Dependence of the gain transistor from of the thickness of the electrically neutral base (a) and from the emitter current I_E, A (b)

Thus, the gain of bipolar nanotransistors is significantly higher than that of similar micro- and submicron analogues due to the reduced influence of the lateral (end) regions of the nanotransistor base on recombination losses. These effects require additional studies of two-dimensional models of nanotransistors.

V. Prospects for Further Research

The obtained results of the technological design of the two-stage process of impurity diffusion in nanoscale structures of bipolar transistors open a number of promising directions for further scientific research.

First, it is advisable to build a model taking into account two-dimensional and three-dimensional diffusion effects, which are of particular importance in the conditions of further reduction of transistor sizes [3]. At such scales, the inhomogeneity of the distribution of impurities over the plane and depth significantly affects the electrical characteristics of devices, and therefore, taking into account the spatial anisotropy of diffusion will allow obtaining more accurate predictions.

Secondly, a promising direction is to take into account the effects of recombination, generation and electrostatic screening in the model [5]. This will allow describing the dynamics of charge carriers during technological stages and in the operating mode of the transistor, which is important for the further transition from topological to fully functional electrophysical modeling.

Thirdly, the obtained results should be integrated into complex CAD systems, in particular by developing software modules for predicting transition parameters at the nanocircuit design stage.

Taking into account the above, further development of technological design of bipolar nanodevices will contribute to the creation of more accurate, reliable and efficient semiconductor structures, oriented to the requirements of modern and promising nanoelectronics.

VI. Conclusion

Thus, the work successfully conducted physical and topological modeling of the process of forming a bipolar nanotransistor using diffusion methods. The main results obtained in the course of the work can be summarized as follows:

The main methods of creating a junction in a silicon substrate using diffusion processes were considered. The features of the sequential introduction of impurities and their influence on the characteristics of the nanotransistor were studied.

Using the MathCad software environment, numerical modeling of the process of diffusion of impurities into a semiconductor substrate was carried out. The dependence of the concentrations of donor and acceptor impurities on the depth of occurrence and the influence of the temperature regime on the final distribution of impurities were studied.

Calculations of the width of the electroneutral base region, the depth of occurrence of the collector

and emitter junctions were performed, which allowed us to estimate the electrophysical parameters of the resulting structure. The influence of diffusion time and temperature on the depth of penetration of impurities was determined.

A series of mathematical experiments were carried out, varying the diffusion time and temperature, which allowed obtaining the optimal parameters for the formation of the proper transistor nanostructure. The results showed that the controlled selection of technological parameters allows achieving the required transistor characteristics.

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О. С. Мельник, В. О. Козаревич, О. О. Нагайченко. Автоматизоване технологічне проєктування нанорозмірних транзисторів

Статтю присвячено автоматизації технологічної підготовки сучасних високочастотних та енергоефективних біполярних транзисторів з нанорозмірними глибинами імплантації домішок в нанопровідникову підкладку. На етапі математичного моделювання технологічних операцій багатошарового легування враховані відомі теоретичні та емпіричні, розроблені авторами статті, високотемпературні залежності параметрів легування, розподіли глибин межевих відстаней емітерного і колекторного переходів, які, в підсумку, визначають товщину електронейтральної базової області транзистора. Запропоновано математичні моделі технологічних параметрів поверхневих та об'ємних концентрацій домішок, які спричиняють виродження та неодноразової інверсії типів провідності початкової кристалічної підкладки. Визначені гранично можливі величини тиктури та розчину акцепторних та донорних домішок, які підвищують коефіцієнти підсилення та зменшують енергоспоживання біполярних нанотранзисторів. Враховані дрейфові складові струмів бази та колектора, які викликані внутрішнім електричним полем неоднорідної бази. Знайдені температурні та часові залежності технологічних операцій легування, які в першу чергу визначають створення біполярннх транзисторів з товщиною бази від 100 нм до 10 нм. Встановлені величини граничних концентрацій домішок напівпровідникових структур. Розглянуті приклади, які підтверджують ефективність запропонованих методів автоматизованого проектування біполярних нанотранзисторів. В подальшому планується розробка узагальнених алгоритмів багаторівневого ієрархічного моделювання компонентів транзисторної наноелектроніки.

Ключові слова: автоматизація технологічної підготовки; транзисторна наноелектроніка; імплантація домішок; електронно-дірковий перехід; електронейтральна база; коефіцієнт підсилення.

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