AUTOMATION AND COMPUTER-INTEGRATED TECHNOLOGIES

UDC 621.382-022.532(045)
DOI:10.18372/1990-5548.82.19377

[1]O. S. Melnyk,
[2]V. O. Kozarevych,
[3]Y. M. Kushnirenko

PROGRAMMED MICRO- AND NANOSTRUCTURES

Department of Electronics, Robotics, Monitoring & IoT Technologies
National Aviation University, Kyiv, Ukraine
E-mails: [1]oleksandr.melnyk@npp.nau.edu.ua, ORCID 0000-0003-1072-5526,
[2]viktoriia.kozarevych@npp.nau.edu.ua, ORCID 0000-0002-4380-0927, [3]5344175@stud.nau.edu.ua

***Abstract*—*The article examines controversial issues regarding the implementation of specialized, but at the same time universal, large integrated circuits, which appear in the initial stages of automated hierarchical design. To increase the efficiency of automated design systems, universal micro- and nanocircuits with programmable logic have been created. The article offers effective methods of programming multiplexer micro- and nanocircuits with programmable logic for implementing Boolean and majority logic functions. The obtained results are used to configure the functional blocks of the multiplexers. With the use of modern automated design systems, comparative modeling of logical micro- and nanocircuits was carried out, which confirmed the adequacy of their work, as well as the advantages of frequency and temperature characteristics of nanomultiplexer circuits.*

Index Terms—Programmable logic structures; micro- and nanocircuits; logical functions; computer-aided design; multiplexer.

I. INTRODUCTION

The programming of micro- and nanomultiplexers does not provide for the possibility of creating algorithms for processing input multi-argument functions by changing work programs, as is usually implemented by microcontrollers. It refers to technological changes in the internal structure of electronic circuits in such a way as to ensure the synthesis of the necessary functions at the structural and logical level.

II. ANALYSIS OF RECENT RESEARCH AND PUBLICATIONS

Research in the field of programmed micro- and nanocircuits is actively developing, and a significant part of the attention of scientists is focused on the automated hierarchical design of such systems. The first significant breakthroughs in this field occurred as a result of the development of multi-structural systems built on the basis of universal functionally complete modules. Such modules turned out to be one of the promising trends in the development of modern electronics [1]. These studies demonstrated the possibility of automated design of micro- and nanocircuits capable of implementing 16 two-argument and 256 three-argument functions based on multiplexers [2]. However, there are significant difficulties in simplifying these schemes, which causes excessive complexity in implementation and their universal application. An important aspect of the research was the improvement of the methods of programming of micro- and nanocircuits for the reproduction of various functions of the algebra of logic [3], [4]. Scientists proposed effective algorithms for automated programming of microcircuits with a high level of integration, which became the basis for the further development of nanodevices with programmable structures [9]. Despite significant progress in this area, the task of achieving effective automated design still remains open, and today the problem of simplifying algorithms and their adequate reproduction is the subject of active discussions.

Special attention should be paid to the influence of temperature regimes on the performance of nanocircuits, in particular, operation at cryogenic temperatures. Studies have shown that such conditions can significantly affect the operation of nanodevices, stimulating the search for new approaches to improve their quality and stability of operation [6]. The issues of synchronizing such schemes also remain unresolved, which creates additional challenges for their implementation. As a result, the issues of improving the quality of micro- and nanocircuits with programmable logic remain relevant and require further research and improvement.

III. PROGRAMMING OF MULTIPLEXER MICRO- AND NANOSTRUCTURES

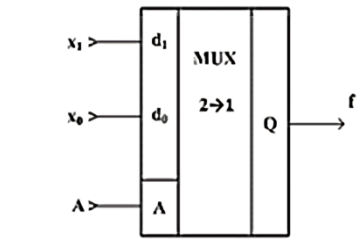
To use multiplexers as universal logical nanocomponents, the signals of some arguments of the reproduced function are fed to the address inputs, and the information inputs play the role of programmable nanostructures. For a digital device with two input variables x_1, x_0, four combinations of arguments are useful: 00, 01, 10, 11, and this allows the implementation of 16 different output functions.

The designation (a) of a multiplexer with two inputs (2→1) is shown in Fig. 1. From the truth table after the transformations, the function of the logic algebra of the multiplexer (2→1) takes the form:

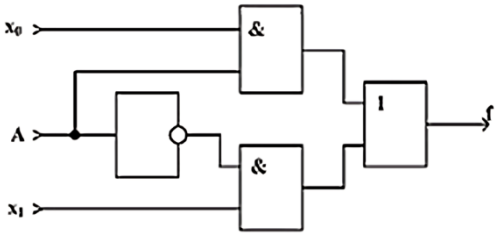
$$f_{\text{MUX}} = \overline{A}D_0\overline{D}_1 \vee \overline{A}D_0D_1 \vee A\overline{D}_0D_1 \vee AD_0D_1 = D_1A \vee D_0A, \quad (1)$$

To reproduce two-argument functions, it is necessary to carry out a transformation to obtain disjunctive normal forms. For example, using de Morgan's duality law (inversion) for the NOR function, we get: $f_1 = \overline{x_1 \vee x_0}$, gets $f_1 = \overline{x}_1\overline{x}_0$, and implement the programming algorithm (1):

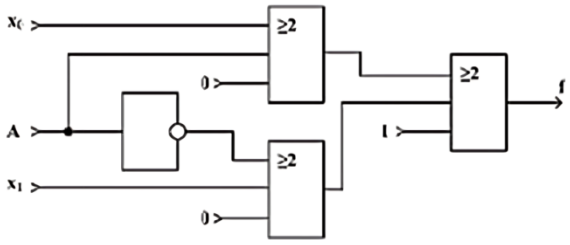
$$f_1 = \overline{x}_1\overline{x}_0 = D_1A \vee D_0\overline{A}\#. \quad (2)$$



a)



b)



c)

A	D_0	D_1	f_{MUX}
0	0	0	$D_0 = x_0 = 0$
0	0	1	$D_0 = x_0 = 0$
0	1	0	$D_0 = x_0 = 1$
0	1	1	$D_0 = x_0 = 1$
1	0	0	$D_1 = x_1 = 0$
1	0	1	$D_1 = x_1 = 1$
1	1	0	$D_1 = x_1 = 0$
1	1	1	$D_1 = x_1 = 1$

d)

Fig. 1. Two-input multiplexer (a), its micro- (b) and nanocircuits (c) and truth table (d)

Then, for four-time programming of one address input with argument constants, it is necessary to apply the following combinations of signals to two information inputs:

$$A = \overline{x}_1, D_1 = \overline{x}_0 D_0 = \overline{x}_1 \text{ or } 0,$$

$$A = x_1, D_1 = \overline{x}_1 \text{ or } 0,\ D_0 = x_0,$$

$$A = \overline{x}_0, D_1 = x_1 D_0 = x_0 \text{ or } 0, D_0 = x_0,$$

$$A = x_0, D_1 = x_0 \text{ or } 0,\ D_0 = x_1,$$

IV. RESULTS AND DISCUSSION

From the above examples, the final programming table of MNCL (2→1) multiplexers for the implementation of 16 two-argument functions is obtained (Table I). According to Fig. 1b, the two-input MNCL was built on the basis of the CAD design system Micro-cap 11 [7] (Fig. 2) from logic elements (a) and from a separate element in one case in the form of a macro diagram (b). In Figure 3 shows a diagram of the computer implementation of the OR function on four MNCLs (a), which are configured according to the transformation (2) and column f 6 from Table I, as well as the results of its simulation (b).

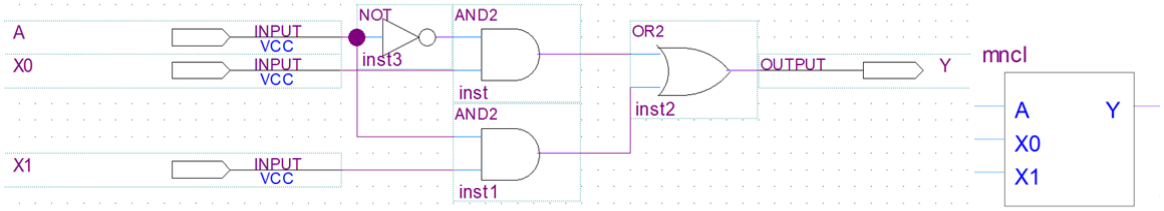
Quantum cellular automata (QCA) is a computing paradigm, according to which information is represented by a certain configuration of electrons in a QCA cell, which is formed from one or two separate molecules [5]. Devices based on this technology consist of nanoscale dielectric cells with four quantum semiconductor dots located at the corners and two mobile electrons.

The previously created MNCL on a two-input nanomultiplexer (Fig. 1c) is built on the basis of

single-electron nanocircuits QCADesigner (Fig. 4a). It consists of an address signal inverter A at the ME input, the structure of which is programmed with a zero polarization of – 1.00 to perform a conjunction (AND) operation, and an ME output, which is structurally programmed with a 1.00 polarization to reproduce the disjunctive logic function f_{MUX} (1). The results of modeling its time diagrams, which completely coincide with the truth Table (Fig. 1d), are shown in Fig. 4b.

TABLE 1. LOGICAL FUNCTIONS OF TWO ARGUMENTS FOR MNCL MULTIPLEXERS (2→1)

Programming options																		
	1	D_0	0	$\overline{x_1}(0)$	$\overline{x_1}(0)$	$\overline{x_1}(0)$	x_0	$\overline{x_1}(0)$	$\overline{x_1}(0)$	$\overline{x_0}$	x_0	x_0	$x_0(1)$	x_0	$x_1(1)$	$x_1(1)$	$x_1(1)$	1
		D_1	0(1)	$\overline{x_0}$	x_0	$\overline{x_1}(1)$	$x_1(0)$	$\overline{x_0}(1)$	x_0	$\overline{x_1}(1)$	$x_1(0)$	$\overline{x_0}$	$x_0(0)$	$\overline{x_1}(1)$	$x_1(0)$	$\overline{x_0}$	x_0	0(1)
		A	0	$\overline{x_1}$	$\overline{x_1}$	$\overline{x_1}$	$\overline{x_1}$	$\overline{x_0}$	$\overline{x_1}$	$\overline{x_1}$	$\overline{x_1}$	$\overline{x_1}$	$\overline{x_0}$	$\overline{x_1}$	$\overline{x_1}$	$\overline{x_1}$	$\overline{x_1}$	0
	2	D_0	0(1)	$\overline{x_0}$	x_0	$\overline{x_1}(1)$	$x_1(0)$	$\overline{x_0}(1)$	x_0	$\overline{x_1}(1)$	$x_1(0)$	$\overline{x_0}$	$x_0(0)$	$\overline{x_1}(1)$	$x_1(0)$	$\overline{x_0}$	x_0	0(1)
		D_1	0	$\overline{x_1}(0)$	$\overline{x_1}(0)$	$\overline{x_1}(0)$	$\overline{x_0}$	$\overline{x_0}(0)$	$\overline{x_0}$	$\overline{x_0}$	x_0	x_0	$x_0(1)$	x_0	$x_1(1)$	$x_1(1)$	$x_1(1)$	1
		A	1	x_1	x_1	x_1	x_1	x_0	x_1	x_1	x_1	x_1	x_0	x_1	x_1	x_1	x_1	1
	3	D_0	$\bar{x}(0)$	$\overline{x_1}(0)$	$\overline{x_1}$	$\overline{x_1}$	$\overline{x_0}(0)$	$\overline{x_0}$	$\overline{x_1}$	$\overline{x_1}$	x_1	x_1	x_0	$x_0(1)$	x_1	x_1	$x_0(1)$	$x(1)$
		D_1	$x(0)$	$\overline{x_1}$	$x_0(0)$	$\overline{x_1}(0)$	x_1	$\overline{x_0}(0)$	x_1	$\overline{x_0}(1)$	$x_0(0)$	$\overline{x_1}$	$x_0(0)$	$\overline{x_1}$	$x_1(0)$	$\overline{x_0}(1)$	x_1	$\bar{x}(1)$
		A	$\bar{x}$	$\overline{x_0}$	$\overline{x_0}$	0	$\overline{x_0}$	0	$\overline{x_0}$	$\overline{x_0}$	$\overline{x_0}$	$\overline{x_0}$	0	$\overline{x_0}$	0	$\overline{x_0}$	$\overline{x_0}$	$\bar{x}$
	4	D_0	$x(0)$	$\overline{x_1}$	$x_0(0)$	$\overline{x_1}(0)$	x_1	$\overline{x_0}(0)$	x_1	$\overline{x_0}(1)$	$x_0(0)$	$\overline{x_1}$	$x_0(0)$	$\overline{x_1}$	$x_1(0)$	$x_0(1)$	x_1	$\bar{x}(1)$
		D_1	$\bar{x}(0)$	$\overline{x_1}(0)$	$\overline{x_1}$	$\overline{x_1}$	$x_0(0)$	$\overline{x_0}$	$\overline{x_1}$	x_1	x_1	x_1	x_0	$x_0(1)$	x_1	x_1	$x_0(1)$	$x(1)$
		A	x	x_0	x_0	1	x_0	1	x_0	x_0	x_0	x_0	1	x_0	1	x_0	x_0	x
0/1	0/1	0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0/1	0/1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
0/1	1/0	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
0/1	1/0	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
1/0	0/1	0	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1/0	0/1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1/0	1/0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
1/0	1/0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
x_1/$\overline{x_1}$	x_0/$\overline{x_0}$	A	$f_0 = 0$	$f_1 = \overline{x_1 \vee x_0}$	$f_2 = \overline{x_1}x_0$	$f_3 = \overline{x_1}$	$f_4 = x_1\overline{x_0}$	$f_5 = \overline{x_0}$	$f_6 = x_1 \oplus x_0$	$f_7 = \overline{x_1 x_0}$	$f_8 = x_1 x_0$	$f_9 = \overline{x_1 \oplus x_0}$	$f_{10} = x_0$	$f_{11} = \overline{x_1} \vee x_0$	$f_{12} = x_1$	$f_{13} = x_1 \vee \overline{x_0}$	$f_{14} = x_1 \vee x_0$	$f_{15} = 1$



a) b)

Fig. 2. Two-input MNCL on microelements (a) and in the macro housing (b)

In addition, the computer design of a one-electron MNCL with a configurable configuration (Fig. 5a compared to Fig. 4a) and the choice of programming for the f_6 XOR function (see Table 1) were carried out:

$$A = x_1, \quad x_1(D_1) = \overline{x}_0$$

and $\quad x_0(D_0) = x_0.$

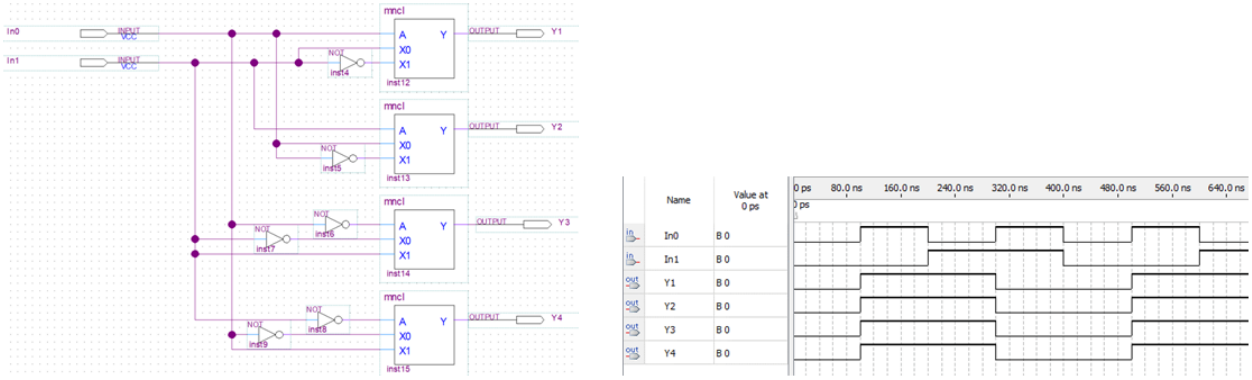
Checking the correspondence between the simulation time diagrams (Fig. 5b) and the truth Table I confirms the adequacy of the adjusted MNCL.

In addition, a comparison of the simulation results of the oscillograms of micro- (Fig. 3b) and nanocircuit (Fig. 5b) multiplexers allows us to conclude that the curves completely match and reliably reproduce the configured XOR logic function.

V. CONCLUSIONS

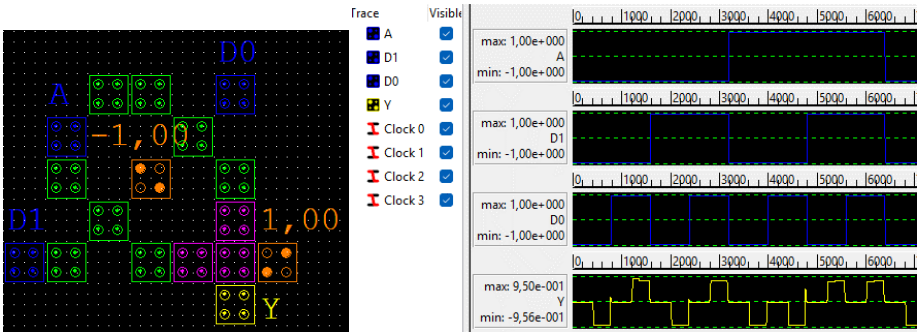
Since the development of microelectronics based on metal-oxide-semiconductor complementary transistors is limited by quantum-technological and small-scale effects, the article gives priority to the

application of nanodevices with programmable structures for the implementation of logic functions. The developed algorithms Table I of the automated modification of MNCL Figs. 3 and 5 confirmed the adequacy of the proposed models. However, the disadvantage of single-electron circuits is the ultra-low temperature range from 0 to 4K of their operation.



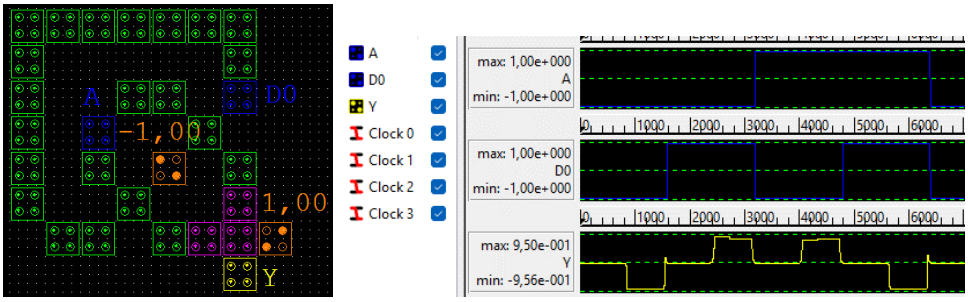
a) b)

Fig. 3. Automated configuration of MNCL (a) and time diagram of the programmed XOR function (b)



a) b)

Fig. 4. Automated programming of the MNCL nanocircuit (a) and corresponding oscillograms (b)



a) b)

Fig. 5. Computer design of the MNCL on the spacecraft: (a) single-argument nanocircuit, (b) results of time simulation

REFERENCES

[1] C. S. Lent and P. D. Tougaw, "A Device Architecture for Computing with Quantum Dots," *IEEE Transactions on Nanotechnology*, vol. 4, no. 4, pp. 49–58, 1997. https://doi.org/10.1109/5.573740

[2] D. Harris and S. Harris, *Digital Design and Computer Architecture: ARM Edition*, Morgan Kaufmann, San Francisco, CA, 2015, 307 p. https://doi.org/10.1016/B978-0-12-800056-4.00006-6

[3] E. Sicard and S. D. Bendhia, *Advanced CMOS Cell Design*, McGraw-Hill, 2007, 385 p.

[4] J. L. Hennessy and D. A. Patterson, *Computer Architecture: A Quantitative Approach*, Morgan Kaufmann, 2011, 856 p.

[5] K. Walus and G. A. Jullien, "Design and Simulation of Quantum-Dot Cellular Automata Circuits," *Journal of Applied Physics*, vol. 99, no. 2, pp. 123–130, 2006.

[6] K. Walus, G. A. Jullien, "Quantum-Dot Cellular Automata: Theory and Application," *IEEE Transactions on Nanotechnology*, vol. 99, no. 2, pp. 123–130, 2006.

[7] N. K. Jha and K. Roy, *Nanoelectronic Circuit Design*, Springer, 2010, 439 p. https://doi.org/10.1007/978-1-4419-7609-3

[8] O. S. Melnyk and V. O. Kozarevych, "Nanodevices with Programmable Logic," *Electronics and Control Systems*, vol. 4, no. 62, pp. 47–52, 2019. https://doi.org/10.18372/1990-5548.62.14383

[9] P. P. Chu, *FPGA Prototyping by VHDL Examples*, Wiley & Sons, 2008, 528 p. https://doi.org/10.1002/9780470231630

[10] S. Birla, S. K. Dargar, and N. Singh, *Low Power Designs in Nanodevices and Circuits for Emerging Applications*, CRC Press, 2022, 452 p. https://doi.org/10.1201/9781003459231

Received August 14, 2024

Melnyk Oleksandr. ORCID 0000-0003-1072-5526. Candidate of Sciences (Engineering). Associated Professor.
Department of Electronics, Robotics, Monitoring & IoT Technologies, National Aviation University, Kyiv, Ukraine.
Education: Kyiv Polytechnic Institute, Kyiv, Ukraine, (1971).
Research interests: Modeling micro- and nanoelectronics devices, computer-aided designe, solid-states electronics.
Publications: more than 170 papers.
E-mail: oleksandr.melnyk@npp.nau.edu.ua

Kozarevych Viktoriia. ORCID 0000-0002-4380-0927. Senior Lecturer.
Department of Electronics, Robotics, Monitoring & IoT Technologies, National Aviation University, Kyiv, Ukraine.
Education: National Aviation University, Kyiv, Ukraine, (2007).
Research interests: Computer-aided design, single-electron circuits, solid-states electronics.
Publications: 35.
E-mail: viktoriia.kozarevych@npp.nau.edu.ua

Kushnirenko Yurii. Student.
Department of Electronics, Robotics, Monitoring & IoT Technologies, National Aviation University, Kyiv, Ukraine.
Education: student of National Aviation University, Kyiv, Ukraine.
Research interests: Computer-aided design, solid-states electronics, internet of things.
Publications: 1.
E-mail: 55344175@stud.nau.edu.ua

О. С. Мельник, В. О. Козаревич, Ю. М. Кушніренко. Мікро- та наносхеми з конфігурованою логікою
У роботі розглянуто актуальні питання щодо впровадження спеціалізованих, але водночас універсальних великих інтегральних схем, які виникають на початкових етапах автоматизованого ієрархічного проектування. Для підвищення ефективності цих систем запропоновано універсальні мікро- та наносхеми з конфігурованою логікою. Представлено ефективні підходи до програмування мультиплексорних мікро- та наносхем для реалізації булевих та мажоритарних логічних функцій. Отримані результати застосовано для налаштування функціональних блоків мультиплексорів. Проведене моделювання мікро- та наносхем за допомогою сучасних систем автоматизованого проектування підтвердило їхню функціональну адекватність, а також виявило переваги частотних і недоліки температурних характеристик наномультиплексорів.
Ключові слова: конфігуровані логічні структури; мікро- та наносхеми; логічні функції; автоматизоване проектування; мультиплексори.

Мельник Олександр Степанович. ORCID 0000-0003-1072-5526. Кандидат технічних наук. Доцент.
Кафедра електроніки, робототехніки, моніторингу та технологій Інтернету речей, Національний авіаційний університет, Київ, Україна.
Освіта: Київський політехнічний інститут, Київ, Україна, (1971).
Напрям наукової діяльності: моделювання пристроїв мікро- та наноелектроніки, автоматизоване проектування, твердотільна електроніка.
Кількість публікацій: більше 170 наукових робіт.
E-mail: oleksandr.melnyk@npp.nau.edu.ua

Козаревич Вікторія Олександрівна. ORCID 0000-0002-4380-0927. Старший викладач.
Кафедра електроніки, робототехніки, моніторингу та технологій Інтернету речей, Національний авіаційний університет, Київ, Україна.
Освіта: Національний авіаційний університет, Київ, Україна, (2007).
Напрям наукової діяльності: системи автоматизованого проектування, одноелектронні схеми, твердотільна електроніка.
Кількість публікацій: 35.
E-mail: viktoriia.kozarevych@npp.nau.edu.ua

Кушніренко Юрій Миколайович. Студент.
Кафедра електроніки, робототехніки, моніторингу та технологій Інтернету речей, Національний авіаційний університет, Київ, Україна.
Освіта: студент Національного авіаційного університет, Київ, Україна.
Напрям наукової діяльності: системи автоматизованого проектування, твердотільна електроніка, Інтернет речей.
Кількість публікацій: 1.
E-mail: 5344175@stud.nau.edu.ua