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# MICRO- AND NANOCIRCUITS WITH CONFIGURABLE LOGIC

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Abstract—The work considers controversial problems with the introduction of specialized and at the same time universal large integrated circuits, which are clarified at the initial stages of automated hierarchical design. Universal micro- and nanocircuits with configurable logic are created in the article to increase the efficiency of automated design systems. The article provides effective methods of programming multiplexer micro- and nanocircuits with configured logic for implementing Boolean and majority logic functions. The obtained results are used to configure the multiplexer functional blocks. With the help of modern automated design systems, comparative modeling of logic micro- and nanocircuits with configured logic was performed, which proved the adequacy of their functioning, the advantages of frequency and disadvantages of temperature characteristics of nanomultiplexer circuits.

**Index Terms**—Configurable logic structures; micro- and nanocircuits; logical functions; computer-aided design; multiplexer.

## I. INTRODUCTION

Configuration (structural programming) of micro- and nanomultiplexers does not mean the ability to create algorithms for processing input multi-argument functions by changing work programs, as is usually implemented by a microcontroller, but technological changes in the internal configurations of electronic circuits in such a way that they provide the synthesis of the necessary functions on a structural – logical level.

# II. ANALYSIS OF RECENT RESEARCH AND PUBLICATIONS

Scientists of the Kharkiv University of Radio Electronics [1] and the American University of Cleveland [2] were the first to propose multistructure micro- and nanosystems based on universal functionally complete modules as one of the most promising areas of electronics development.

Recently, research and results of automated hierarchical design of configurable micro- and nanocircuits have been sufficiently fully described in domestic and foreign publications [3] – [11]. There are many technical problems in which it is possible to implement 16 two- and 256 three-argument functions based on multiplexers within the framework of non-automated configurable [3] – [5] of micro- and nanocircuits. However, as a universal logical microelement, such implementations are redundant in advance. In addition, it is assumed that such schemes are fault-tolerant. The works of the authors of this

article [6], [7] were devoted to solving these problems, but in practice the goal of automated design of microand nanocircuits with configurable logic (MNCL) has not yet been achieved.

In works [7], [8], the researchers proposed effective methods of configuring micro- and nanodevices to reproduce a wide range of functions of the logic algebra of combinational and sequential devices. The publication [7] presents an algorithm for automated programming of microcircuits with a high degree of integration, which is partially reproduced in this article for nanoelectronic devices with programmable structures.

In the monographs [8] and [9], circuit models and their programming algorithms are substantiated, but the possibility of multivariate simplification approaches and their adequate implementations is not proven.

This article proposes multi-level procedures for monitoring the results of configuration micro- and nanocircuits. The issues of synchronization and the influence of cryotemperatures on the performance of nanodevices have not yet been sufficiently investigated [3], [6], [11], therefore they stimulate the further search for additional approaches to improve the quality of MNCL.

The purpose of the work is to introduce computer aided methods of modeling and designing multiplexer micro- and nanocircuits with configurable structures for the implementation of logical functions of Boolean and majority algebrath.

The operating characteristics of MNCL are worse in advance than those of standard microcircuits.

# III. PROGRAMMING OF MULTIPLEXER MICRO- AND NANOSTRUCTURES

To use multiplexers as a universal logical nanoelement, the signals of some arguments of the reproduced function are switched to its address inputs, and the information inputs perform the role of programmable nanostructures. For a digital device with two input variables  $x_1$ ,  $x_0$ , four possible combinations of arguments are possible: 00, 01, 10, 11 and 10 and 16 different output functions.

Figure 1 shows the conventional designation (a) of the multiplexer  $(2\rightarrow 1)$ .

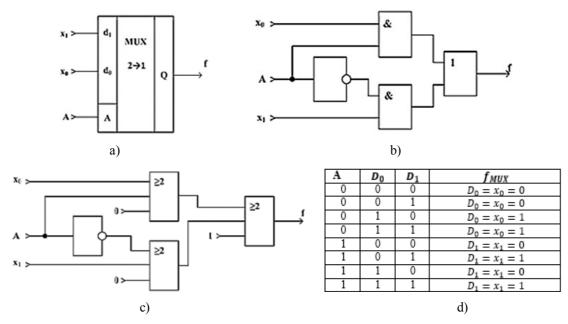


Fig. 1. Two-input multiplexer (a), its micro- (b) and nanocircuits (c) and truth table (d)

From the table in Fig. 1d, after parenthesis transformations, the function of the logic algebra of the multiplexer  $(2\rightarrow 1)$  is obtained:

$$f_{\text{MUX}} = \overline{A}D_0\overline{D}_1 \vee \overline{A}D_0D_1 \vee A\overline{D}_0D_1 \vee AD_0D_1$$

$$= D_1A \vee D_0\overline{A}. \tag{1}$$

To reproduce two-argument functions transformations must be performed to obtain disjunctive normal forms. Yes, using de Morgan's law of duality (inversion) for the NOR function  $f_1 = \overline{x_1 \vee x_0}$ , gats  $f_1 = \overline{x_1} \overline{x_0}$ , and implement the programming algorithm (1):

$$f_1 = \overline{x}_1 \overline{x}_0 = D_1 A \vee D_0 \overline{A}. \tag{2}$$

Then, with four-time programming of a single address input by argument constants the following combinations of signals should be applied to the two information inputs:

$$A = \overline{x}_1, D_1 = \overline{x}_0, D_0 = \overline{x}_1 \text{ or } 0,$$

$$A = x_1, D_1 = \overline{x}_1 \text{ or } 0, D_0 = x_0,$$

$$A = \overline{x}_0, D_1 = x_1, D_0 = x_0 \text{ or } 0, D_0 = x_0,$$

$$A = x_0, D_1 = x_0 \text{ or } 0, D_0 = x_1.$$

## IV. RESULTS AND DISCUSSION

From the examples considered above, the final table of programming of MNCL multiplexers  $(2\rightarrow 1)$  is obtained for the implementation of 16 two-argument functions (Table I).

According to Fig. 1b, the two-input MNCL is built on the design area of CAD Micro-cap 11 [9] (Fig. 2) from logical elements (a) and from a separate element in one housing in the macro (b).

Figure 3 illustrates the scheme of the computer implementation of the OR function on four MNCL (a), which are configurable according to transformation (2) and column  $f_{14}$  from Table I and its simulation results (b).

Quantum cellular automata (CA) is a computing paradigm, according to which information is represented by a certain configuration of electrons in the cell of the CA, which is formed from one or two separate molecules [10], [11]. The devices on the spacecraft consist of nano-sized dielectric cells that have four quantum semiconductor dots located in the corners and two mobile electrons.

The previously created MNCL of the two-input nanomultiplexer (Fig. 1c) is built on the QCADesiner single-electron nanocircuits [12] in

Fig. 4a. It consists of an address signal inverter A, two input MEs, the structures of which are programmed with zero polarizations - 1.00 to perform the conjunction operation AND, and the output ME structurally programmed with a single

TABLE I.

polarization of 1.00 to reproduce the disjunctive output logic function  $F = f_{MUX}$  (1). Fig. 4b shows the results of modeling its time diagrams, which completely coincide with the truth table (Fig. 1d).

1	x <sub>1</sub>	x <sub>0</sub>			/ x <sub>0</sub>	Хo	Let	<u>x</u> 0	ľė	D x0	<u>x</u> 0	χo	θ x <sub>0</sub>	r <sub>o</sub>	ν x <sub>0</sub>	1,	٧ <del>٪</del> ٥	
I	/	/	A	0 =	x1 v	12	x	x <sub>1</sub> 3	½	Φ.	χ <sub>1</sub> ,	x13	1 th	× =	12	*	1,1	

LOGICAL FUNCTIONS OF TWO ARGUMENTS FOR MNCL MULTIPLEXERS (2→1)

 $f_{14} = x_1 \vee x_0$ II  $f_{15}$ îì 400 to S Ш 40 Ť, J. £, 4 Ę  $f_{13}$ ... 0 0 1 0 1 0 1 0 0 0 1 0 1 0 1 1 0 0 1 0 1 0 1 1 0 0 1 0 1 1 0 0 0 0 1 0 0 1 0 1 0 1 1 1 1 1 0 0 0 1 0 0 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 1 0 0 0 0 1 1 1 0 0 0 0 1 1 1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 0 0 0 0 0 0 0 0  $\overline{x_1}(0)$  $\overline{x_1}(0)$  $\overline{x_1}(0)$  $x_0$  $\overline{x_1}(0)$  $\overline{x_1}(0)$  $\overline{x_0}$  $x_1(1)$  $x_1(1)$  $x_0$  $x_0$  $x_0(1)$  $x_0$  $x_1(1)$ 1 0(1)  $\overline{x_0}$ 0(1)  $\overline{x_0}$  $\overline{x_1}(1)$  $x_1(0)$  $x_1(0)$  $x_0(0)$  $x_1(0)$  $x_0$  $\overline{x_0}(1$  $x_0$  $\overline{x_1}(1$  $x_0$  $\overline{x_1}(1$  $x_0$ Programming options 0 Α  $\overline{x_1}$ 0  $\overline{x_1}$  $\overline{x_1}$  $\overline{x_1}$  $\overline{x_1}$  $\overline{x_0}$  $\overline{x_1}$  $\overline{x_1}$  $\overline{x_0}$  $\overline{x_1}$  $\overline{x_1}$  $\overline{x_1}$  $\overline{x_1}$ 0(1) 0(1)  $\overline{x_0}$  $\overline{x_1}(1)$  $x_0$  $\overline{x_0}$  $x_0$  $x_0$  $x_1(0)$  $\overline{x_0}(1$  $\overline{x_1}(1$  $x_1(0)$  $x_0$  $x_0(0)$  $\overline{x_1}(1$  $x_1(0)$ 0  $\overline{\chi_1}(0)$  $\overline{x_1}(0)$  $\overline{x_1}(0)$  $\overline{x_0}$  $\overline{x_0}(0)$  $\overline{x_0}$  $x_0$  $x_0(1)$  $x_0$  $x_1(1)$  $x_1(1)$  $x_0$ 1  $\overline{A}$ 1  $x_1$  $x_0$  $x_1$  $x_1$  $x_1$  $x_1$  $D_o$  $\bar{x}(0)$  $\overline{x_1}$  $\overline{x_1}$  $\overline{x_1}(0)$  $\overline{x_1}$  $\overline{x_0}(0)$  $\overline{x_0}$  $\overline{x_1}$ x(1) $x_0$  $x_0(1$  $x_1$  $x_0(1)$ 3  $D_{I}$  $\overline{x_1}$  $\overline{x_0}(1$  $\bar{x}(1)$ x(0) $x_0(0)$  $\overline{x_1}(0)$  $\overline{x_0}(0)$  $x_0(0)$  $\overline{x_1}$  $\overline{x_1}$  $x_1$  $\overline{A}$ 0  $\overline{x_0}$  $\overline{x_0}$  $\bar{x}$  $\overline{x_0}$  $\overline{x_0}$  $\overline{x_0}$  $\overline{x_0}$  $\overline{x_0}$  $\overline{x_0}$  $\bar{x}$  $D_0$  $\overline{x_1}$  $\overline{x_1}(0)$  $\overline{x_0}(0)$  $\overline{x_1}$ x(0) $x_0(0)$  $x_1$  $\overline{x_0}(1$  $x_0(0)$  $\overline{x_1}$  $x_0(0)$  $x_1(0)$  $x_0(1$  $\bar{x}(1)$  $x_1$  $x_1$  $D_I$  $x_0(0)$  $x_0(1)$  $x_0(1)$  $\bar{x}(0)$  $\overline{x_1}(0)$  $\overline{x_1}$  $\overline{x_1}$  $\overline{x_0}$  $\overline{x_1}$  $x_1$ x(1) $x_1$  $x_1$  $x_0$  $x_0$ 

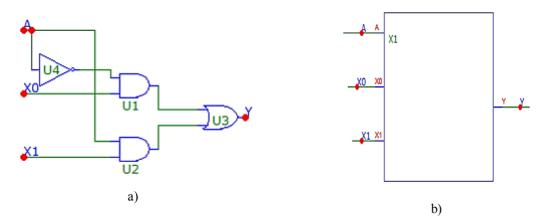


Fig. 2. Two-input MNPS on microelements (a) and in the macro housing (b)

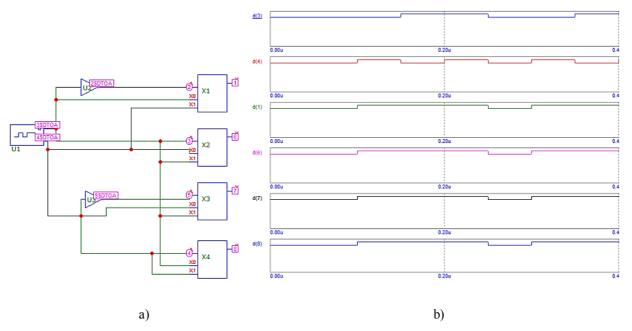


Fig. 3. Automated configuration of MNCL (a) and time diagram of the programmed OR function (b)

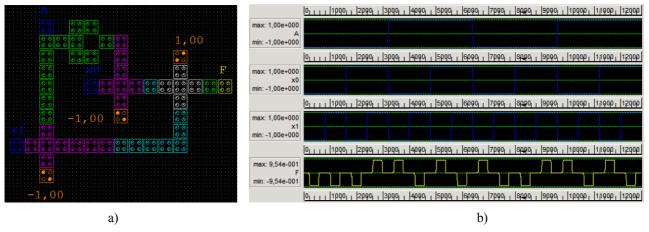


Fig. 4. Automated programming of the MNCL nanocircuit (a) and corresponding oscillograms (b)

Computer design of a single-electron MNCL is performed with configurable adjustment (Fig. 5a compared to Fig. 4a) and selection of programming according to the 4th option for function  $f_{14}$  OR (see Table I):

$$A = x_0, x_1(D_1) = x_0$$
 and  $x_0(D_0 = x_1)$ .

Verification of the correspondence of time modeling (Fig. 5b) and truth Table I confirms the adequacy of the configured MNCL.

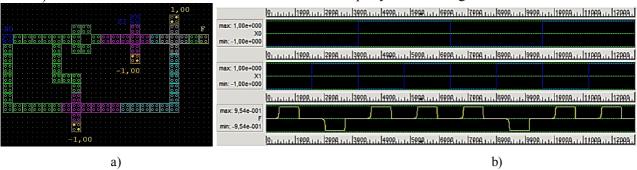


Fig. 5. Computer design of the MNCL on the spacecraft: (a) single-argument nanocircuit, (b) results of time simulation

In addition, a comparison of the simulation results of oscillograms of micro- (Fig. 3,b) and nano-sized (Fig. 5,b) multiplexers allows us to conclude that the curves completely match and reliably reproduce the configurable OR logic function.

# V. CONCLUSIONS

Since the development of microelectronics based on complementary metal-oxide-semiconductor transistors is limited by quantum-technological and small-scale effects [3], the article gives priority to the application of nanoelectronic programmable structures for the implementation of logic functions. The developed algorithms (Table I) of the automated modification of the MNCL (Figs. 3 and 5) confirmed the adequacy of the developed models. However, the disadvantage of single-electron circuits is the supercryogenic temperature range (from 0 to 4K) of operation [10], [11].

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## О. С. Мельник, В. О. Козаревич, М. В. Буток. Мікро- та наносхеми з конфігурованою логікою

У роботі розглянуто суперечливі проблеми із запровадженням спеціалізованих і водночас універсальних великих інтегральних схем, які з'ясовується на початкових етапах автоматизованого ієрархічного проектування. Для підвищення ефективності систем автоматизованого проектування в статті створені універсальні мікро- та наносхеми з конфігурованою логікою. У статті наведено ефективні методи програмування мультиплексорних мікро- та наносхем з конфігурованою логікою для реалізації функцій булевої та мажоритарної логіки. Отримані результати використовуються для конфігурування мультиплексорних функціональних блоків. За допомогою сучасних систем автоматизованого проектування виконано співставне моделювання логічних мікро- та наносхем з конфігурованою логікою, яке довело адекватність їх функціонування, переваги частотних і недоліки температурних характеристик наномультиплексорних схем.

**Ключові слова:** конфігуровані логічні структури; мікро- та наносхеми; логічні функції; автоматизоване проектування; мультиплексори.

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