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STABILITY PARAMETERS OF REGISTER FILE BIT CELL WITH LOW POWER CONSUMPTION PRIORITY

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Abstract*—This research is dedicated to a transistor sizing method of an 8-transistor register file static random access memory bit cell aiming to create two-port register files and two-port static random access memory with reduced supply voltage to reduce power consumption. This method can also be applied to 6-transistor single-port static random access memory bit cells. The method is based on the analysis of butterfly curves and the search for such values of the sizes of transistors and margin of their threshold voltages, in which, for a given critical minimal supply voltage, the condition for the existence of one intersection and one touch of its curves is achieved for the butterfly curves. The obtained samples of the register file bit cells in silicon and its critical voltage were compared to the results of circuit simulation in the write and read mode depending on the supply voltage. Experimental register file chip samples were successfully tested in silicon at a voltage of 0.70-1.8 V.*

Index Terms—Memory bit cell; memory compiler; butterfly curve; register file; power consumption; static noise margin.

I. INTRODUCTION

The development of modern microchip systems (System-on-Chip-SoC) is based on the application of high-level languages, such as RTL Verilog, for simulation, synthesis, placement of blocks and their routing. However, the blocks themselves are library elements, the layout of which is created manually. For example, the logic library for 130nm technology contains more than 150 logic elements, which is considered a satisfactory value. Also, the layout of input/output blocks with different load capacity and functionality, but with the same dimensions, is made manually. It is also worth mentioning parameterized cells (Pcell) – parameterized elements that allow obtaining layouts of individual devices, such as lightly-doped-drain MOS, for which the number of input layers can be more than 30, setting such parameters of transistors as their length and width. Memory compilers belong to a class of industry-specific software that manages parameterized objects, which allows generating and obtaining memory layouts with specified parameters and sizes for use as a library element for further SoC creation. Such compilers are based on a manually developed library of elements and a set of basic memory blocks, such as row and word decoders, control blocks, input and output blocks, and many others.

In some cases, a special requirement is defined on such a parameter of memory instances as the power consumption. This is especially important for autonomous battery-powered systems (such as various sensors, antennas, radars, etc.) that allow for increased uptime. The most effective method of reducing power consumption is to reduce the supply voltage. This approach is particularly effective for 180 nm technology, in which the standard core voltage is 1.8 V. Despite the fact that currently leading semiconductor foundries (fab) have reached design level of 5–7 nm, with the reduction of design standards, the cost of lithography, photo masks and silicon wafers themselves increased dramatically. The 180 nm technology is probably the first production technology that has got two thicknesses of the gate oxide in the standard version, which allows for matching the memory core with a voltage of 1.8 V with the periphery – external circuits with a supply voltage of 3.3 V or 5 V. The cost of photo masks for them and the price of silicon wafers is much cheaper than for advanced nodes. In addition, some fabs offer different options layout scaling during the production. For example, the TSMC factory (Taiwan) offers for its own 180 nm technology scaling in the production process with a factor of 0.84, which allows to reduce the size of the microchip by 30% and reduce the price of the end user product.

However, reducing the supply voltage raises the question of the ability of the memory bit cell to reliably store information in the save and read mode. This is primarily due to variations in the threshold voltage of MOSFET transistors and the dependence of these variations on the size of the transistors of the bit cell itself. In the scientific literature, this effect is called static noise margin (SNM) [1]. The SNM of the memory bit cell is determined graphically as the length of the side of the square

with the largest diagonal in the areas of the butterfly curves (BC) from the bottom right and top left for a symmetrical bit cell, without taking into account the margin of the threshold voltages of the inverters. It is accepted that SNM is equal to the minimum value of the constant noise voltage required to switch the logical state of the bit cell and characterizes the stability of data storage in the register file (RF) or static random access memory (SRAM) bit cell [7] – [10].

II. The Analysis of Memory bit Cell Stability

The precharge of the data buses will be carried out through *n*-channel transistors to a voltage of approximately (*Vdd – Vth*), where *Vth* is the limit voltage of *n*-channel transistors. Since one of the buses of the cell will always be discharged, this approach allows to reduce the consumption current by 10% or more [6].

We will define the margin of static noise as the minimum noise voltage present on each of the gates of the bit cell transistors and associated with the margin of their threshold voltages, which is necessary for switching the state of the cell in the read mode. As the simulation results showed, the margin of static noise directly related to the spread of transistor channel lengths practically does not affect the value of SNM and will not be taken into account further. By itself, the value of SNM without taking into account the margin of the threshold voltage, obtained on the basis of butterfly curves [7] – [9], is not very informative and does not give an idea of whether this value is sufficient for the reliable operation of the bit cell. We will apply the approach related to the analysis of the presence of three points of intersection of the curves and the simultaneous accounting of the influence of the spread of threshold voltages. Butterfly curves will be drawn as a dependence of the output voltage of the first inverter *QN* of the memory cell on the input voltage *Q* and the input voltage *Q* on the output voltage of the second inverter *QN*1. These two inverters have opposite power supply connections simulating the margin of threshold voltages. For one inverter, they are connected to the gate with a positive pin, for the other with a negative pin. This connection option represents worst case.

The basis of the approach will be method 6 σ based on the assumption that the distribution of threshold voltages is Gaussian distribution. With the margin value of the parameter 6 σ and keeping the three points of intersection of the butterfly curves of the diagram, the correct operation of the memory chip is guaranteed at the specified minimum supply voltages.

As a rule, factories in the specifications for their technologies do not provide such parameters as the mean square deviation for the Gaussian distribution, so we will use the data from works [1] – [3]:

$$\sigma(V_t) = AV_t / \sqrt{(2W \times L)}, \quad (1)$$

where $\sigma(V_t)$ is the root mean square deviation of the threshold voltage of a transistor with arbitrary dimensions, AV_t is the root mean square deviation of the threshold voltage of a transistor with dimensions $W = L = 1$ μm. Data for the values of Avt are given in [4], [5] depending on the technology and thickness of the sub-gate oxide. For the technology under consideration, for core transistors with a voltage of 1.8 V, the oxide thickness for the worst case is 4.2 nm, and we have the value $AV_t = 4.51$ mV for an *n*-channel transistor and $AV_t = 5.63$ mV for an *n*-channel transistor.

Further consideration will be conducted for the 180 nm technology of the TSMC fab with a scaling factor $S = 0.84$ at the production stage to the level of 152 nm. To do this, we introduce the scaling factor *S* into equation (1)

$$\sigma(V_t) = AV_t / \sqrt{(2W \times L \times S^2)}. \quad (2)$$

It is important to note that the use of analytical expressions for determining the value of SNM is undesirable for the reason that the SPICE models of transistors provided by fabs are too complex and allow obtaining fairly accurate results, which are caused by their simplification of obtaining analytical solutions. Bit cells analysis for different conditions showed that the worst option is obtained for the case of maximum temperature and section of the fs model – the minimum threshold voltage of *n*-channel transistors and the maximum value of the threshold voltage of *p*-channel transistors. The maximum temperature will be +125º C.

Figures 1 and 2 show the schematic view of the memory bit cell for the two-port register file and its layout.

The bit cell consists of 8 transistors and serves 2 ports – one port for writing, the second port for reading data. The write and read ports are independent and each has its own row and column decoder, its own control blocks. When searching for the necessary solutions, it is necessary to take into account the fact that the value of SNM in the reading mode is affected by the margin of the threshold voltages of all transistors of the cell without exception. Therefore, to simulate the matching effect of transistor parameters, we will use separate voltage

sources on the gates of transistors, the value of which depends on their size according to expression (2). On Figure 3 shows one arm of the inverter with voltage sources that simulate the margin of the threshold voltage.

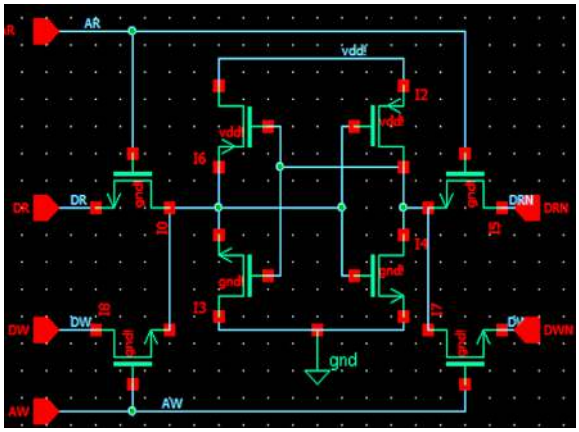

Fig. 1. Schematic view of RFSRAM bit cell

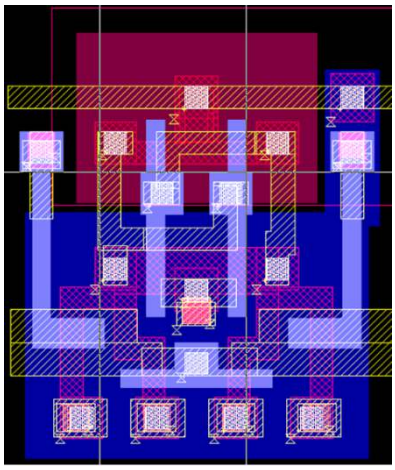

Fig. 2. Layout view of RFSRAM bit cell

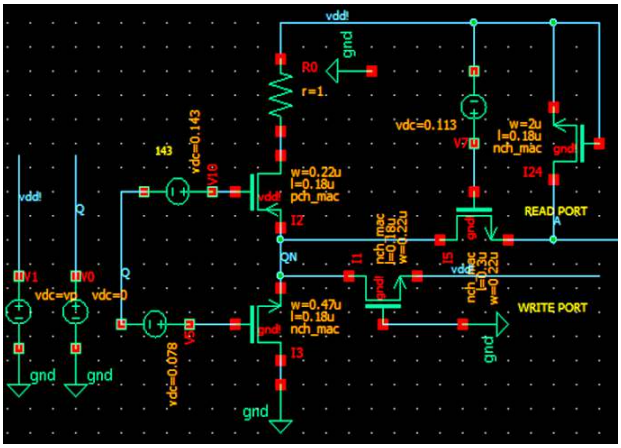

Fig. 3. Electrical circuit for simulation of threshold voltage margin

The second arm is completely similar to the first, except that fact that voltage sources are connected to the gates inversely. In the read mode we are investigating, the address transistor of the write port is closed and its gate is connected to ground. In addition to bit cell transistors, *n*-channel pre-charge transistors are connected to the read bus port, as the purpose is to limit the read bus charge voltage in order to reduce power consumption. This limitation can be applied only for the memory instances with a relatively small number of rows – no more than 64. For a larger number of rows with an increase in the capacity of the data bus, the precharge must be done through *p*-channel transistors – and to the supply voltage level, since the decrease in maximum operating frequency is possible at minimum supply voltages.

Simulation results show that the *n*-channel transistors of memory bit cell inverters exert the maximum influence on cell stability. In addition, judging by the cell layout, a change in the size of the *p*-channel load transistors is possible only in the direction of increasing the channel length, which will lead to an unnecessary local increase in the size and area of the bit cell itself. Table 1 shows the dependence of the value 6 σ for the *n*-channel inverter transistor of the memory bit cell, depending on the channel width and the channel length of 0.18 μm.

TABLE I. DEPENDANCE OF 6 σ ON *W* FOR BIT CELL NMOS WITH *L* = 0.18 μm

***W*, μm**	0.25	0.35	0.45	0.5
6 σ, mV	107.3	90.8	80	75.9

The address transistors of the write port are selected equal to *W* = 0.22 μm, *L* = 0.3 μm and 6 σ = 0.088 V. The channel length of the address transistor is chosen to be greater than the minimum in order to somewhat reduce the threshold voltage margin without increasing the size of the memory bit cell itself. The load *p*-channel transistor is designed with a minimum channel length and width, and has a threshold voltage margin of 6 σ = 0.143 V target value of the minimum supply voltage for butterfly curves analysis is *Vdd* > 0.6 V.

Some results of the BC calculation are shown on Figs 4 and 5 for a supply voltage of 0.6 V. Figure 4 shows the BC for a *n*-channel inverter transistor of a memory cell with a channel width of 0.25 μm.

It can be seen from Fig. 4 that the voltage curves on BC have only one point of intersection in the bottom right corner and therefore the bit cell is unstable in the reading mode. After having conducted a series of simulations, the width of the *n*-channel transistor of the inverter was found to be *W* = 0.47 μm, which has one point of intersection and one point of touching of the curves in the top left corner of the butterfly curves (Fig. 5).

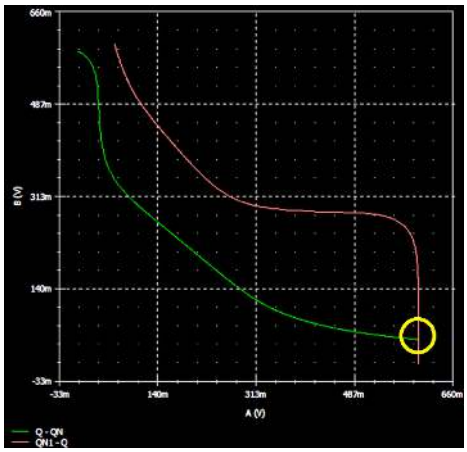

Fig. 4. BC for NMOS of bit cell, V_{dd} = 0.6 V, W = 0.25 μm

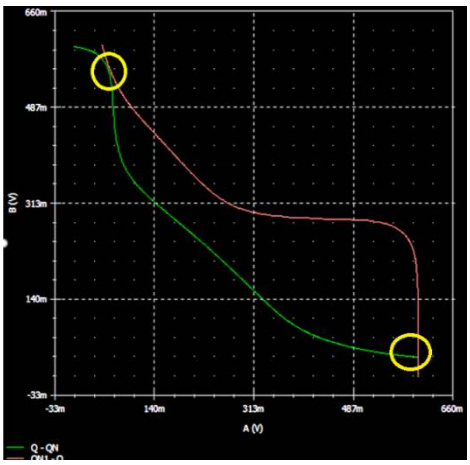

Fig. 5. BC for NMOS of bit cell, Vdd = 0.6 V, W = 0.47 μm

Such a supply voltage of 0.6 V is critical for the bit cell. For all voltages greater than 0.6 V, BC will have 3 intersecting points, and this means that the memory bit cell will be stable from the standpoint of reliable saving information in read mode. Figure 6 shows BC for a supply voltage of 0.65 V, where three points of intersection of the curves are visible pretty good.

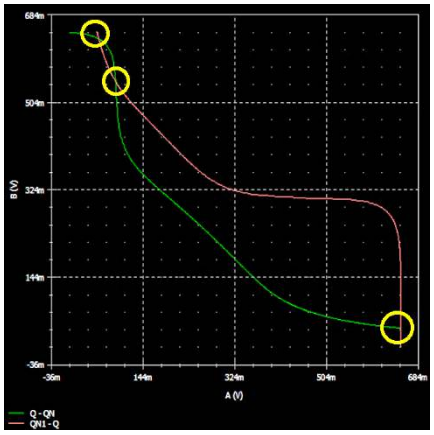

Fig. 6. BC for NMOS of bit cell, V_{dd} = 0.65 V, W = 0.25 μm

III. Comparison with the Results of the Memory Model Calculation

The verification of the obtained results using the instance of a register file with a 20x42 configuration: 20 rows and 42 columns with one port for writing and one for reading. Its schematic view contains all the blocks in its composition, including some parasitic capacitors and resistors. To test the effect of only the threshold voltage margin, the parasitic capacitances between the write and read port data buses in that RF instance have been eliminated. It is mainly because they contribute to additional obstacles in the read mode unrelated to SNM, since the data on the write ports can arrive independently of the read mode. In the bit cell, power sources simulating the margin of the threshold voltage were included, as shown in Fig. 7.

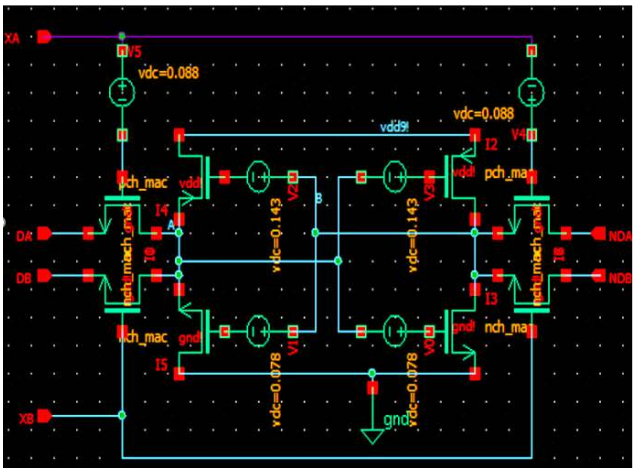

Fig. 7. Bit cell with connected sources

The simulation was conducted for different values of supply voltages. At a critical supply voltage of 0.6 V, loss of information was observed in the reading mode. Figure 8 shows signal diagrams on the internal nodes of the memory bit cell.

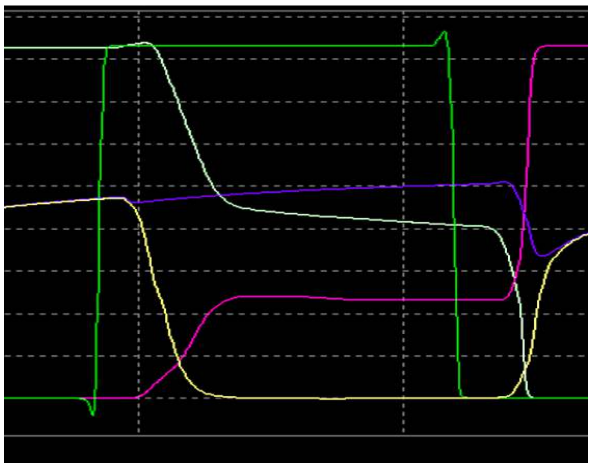

Fig. 8. Diagram of bit cell signals for 0.6 V operating mode

It can be seen that the light green and red curves change their state to inverse after the end of the read operation at the current address. Figure 9 shows the simulation results of the same memory cell at a supply voltage of 0.65 V.

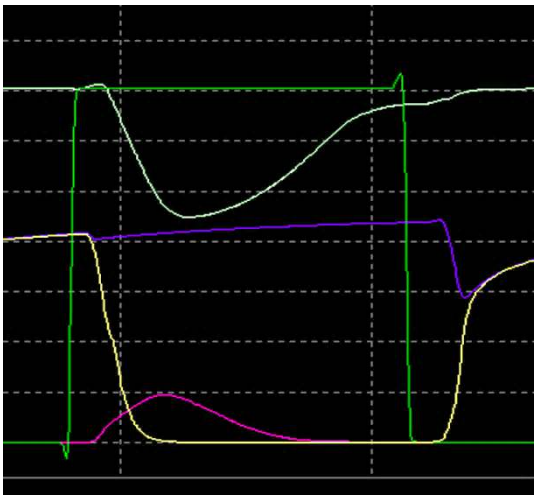

Fig. 9. Diagram of bit cell signals for 0.66 V operating mode

At this value of the voltage, there is no loss of information and it can be seen that the bit cell returns to its state after the end of the reading mode at the current address. It should be noted that the critical voltage depends on the precharge voltage. In case of precharging the data buses to a supply voltage of more than 64 lines, the critical voltage increases to 0.66 V. In other words, the critical supply voltage increases as the increase in the precharge voltage of the data buses.

It can be concluded that the influence of threshold voltage margin on the stability of information retention at critical supply voltages is validated by the simulation results of the register file in the read mode, but without taking into account the influence of parasitic capacitive connections between the data buses of the read and write ports. The loss of information by the memory cell occurs after the end of the read cycle at the current address at critical values of the supply voltage and the margin of the threshold voltages equal to 6 σ. The simulation results have a very good correlation with the results of graphical calculation on butterfly curves.

IV. Calculation of Consumption Currents

Let's calculate the currents and power consumption for the same RFSRAM 20x42 memory instance that was generated by the experimental register file memory compiler. This memory instance was custom designed and subsequently customer manufactured and successfully tested it in silicon at minimum supply voltage of 0.75 V. The simulation will be carried out with the extraction of spicenl.lib netlist files, which we extract from the circuit layout using the SmartDRC/LVS physical verification tool developed by Silvaco, Inc. (USA) for two cases – (1) with parasitic capacitances of layout dilution layers (polysilicon, metals and contacts); (2) without parasitic capacitances. Extraction of parasitic capacitances was carried out for the worst case of minimum dielectric thicknesses between conductive layers and maximum thickness of conductive layers. Under such conditions, parasitic capacitances will be maximum. When extracting parasitic capacitors, their minimum capacity was limited to 1e–16F. The spicenl.lib files generated under such conditions for RFSRAM 20x42 implementation contain 10348 transistors and 8996 parasitic capacitors. For generation, a layout scaling factor of 0.84 was set for both transistor parameters and parasitic capacitances. Simulations of current consumption was carried out at a frequency of 20 MHz for the ambient temperature: minus 40º C (section of ss models) and +125º C (section of fs models). The simulation results are shown in Tables II and III.

TABLE II. F = 20 MHz, T = -40º C, SECTION "SS"

***Vdd*, V**	**0.7**	**0.8**	**1**	**1.8**
Without parasitic capacitances, µA	45	48.6	54.8	113.8
With parasitic capacitances, µA	66	76.2	97.1	170.5
Without parasitic capacitances, µW	31.5	38.9	54.8	204.8
With parasitic capacitances, µW	46.2	61	97.1	306.9

TABLE III. F = 20 MHz, T = +125º C, SECTION "FS"

***Vdd*, V**	**0.7**	**0.8**	**1**	**1.8**
Without parasitic capacitances, µA	52.3	63.4	80.3	158.1
With parasitic capacitances, µA	78.1	90.3	119.3	233.5
Without parasitic capacitances, µW	31.5	38.9	54.8	204.8
With parasitic capacitances, µW	46.2	61	97.1	306.9

As can be seen from these tables, the current consumption and power consumption decrease as the supply voltage decreases. So, for supply voltages of 1.8 V and 0.8 V, the power consumption differs by more than 5 times. It is very important to take into account the influence of parasitic capacitances,

which increase the power consumption by approximately 1.5 times. Table IV shows the results of precharge current calculations for this register file memory instance.

TABLE IV. $F = 20$ MHz, $T = -125^{o}$ C, SECTION "FS"

***Vdd*, V**	**0.7**	**0.8**	**1**	**1.8**
Precharge voltage *Vdd*, µA	15.1	18.5	21.2	38.2
Precharge voltage (*Vdd*, – *Vth*), µA	10.2	11.6	15.1	29.1

For a supply voltage of 0.8 V, the precharge current to the supply voltage is 1.6 times greater than to the voltage (*Vdd – Vth*).

V. CONCLUSIONS

Developed the new approach for determining the transistor sizes of an 8-transistor cell for design of two-port register file and two-port SRAM with reduced supply voltage aiming to reduce power consumption. The new method of determining the minimum supply voltage for 8-transistor and 6-transistor memory cells has been developed. It helps to maintain the reliable operation of the bit cell in read mode with information retention.

Based on the conducted research it is possible to conclude the following.

1) When performing simulation of the margin of the threshold voltage of the all memory bit cell transistors, the voltage sources were included in the butterfly curves calculation scheme.

2) The method based on the graphical analysis of butterfly curves was proposed. The goal of finding such design solutions that preserve the three points of intersection of its curves has been successfully addressed.

3) The concept and meaning of the "critical" supply voltage is introduced, at which there is only one point of intersection and one point of touching of the curves.

4) Performed comparison of the obtained simulation results of the memory instance with the test results of production RF memory samples in silicon. It was conducted in both read and write mode and showed a very good correlation with the results obtained for the butterfly curves regarding the reliability of the memory cell at supply voltages above the critical value.

5) The obtained results showed that for the accurate simulation of currents consumption it is necessary to use the extracted spicenl.lib netlist, taking into account the parasitic capacitances, that in their turn were obtained considering the scaling factor at the manufacturing stage.

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О. М. Груданов. Параметри стабільності комірки регістрового файлу із пріоритетом низького енергоспоживання

Дослідження присвячено методу визначення розмірів транзисторів 8-транзисторної комірки регістрового файлу статичної пам'яті для створення двопортових регістрових файлів і двопортової статичної оперативної пам'яті із зниженою напругою живлення для зменшення споживаної потужності. Цей метод можна застосовувати і для 6-транзисторних комірок однопортових статичних оперативно-запам'ятовуючих пристроїв. Метод засновано на аналізі так званих батерфляй кривих і пошуку таких значень розмірів транзисторів та розкиду їх порогових напруг, за яких, для заданої критичної мінімальної напруги живлення, досягається умова існування одного перетину та одного дотику її батерфляй кривих. Проведено порівняння отриманих зразків пам'яті у кремнії та її критичної напруги з результатами моделювання схеми в режимі запису та читання залежно від напруги живлення. Експериментальні зразки пам'яті успішно пройшли тестування за напруги 0.7–1.8 В.

Ключові слова: комірка пам'яті; компілятор пам'яті; батерфляй крива; регістровий файл; споживання енергії; статичний запас завадостійкості.

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