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SINGLE-ELECTRONIC MULTI-LEVEL ADDERS

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Abstract*—Since metal-oxide-semiconductor microelectronic structures have reached small-scale and quantum limitations, technological models of single-electron nanocircuits of multi-level adders have been created in the work. It has been proven that one bit of information can be encoded by the presence or absence of one electron on a quantum island cluster.This paper provides a simulation of a 4×4 multiplier circuit on the proposed one-bit full adder. As a result, a comparison with other adders was made, an analysis of energy dissipation depending on temperature and the dissipated power of the existing and proposed multipliers in nW was carried out. As a result, it was found that the proposed adder has better properties compared to similar ones. As a result of the work, the simulation of the 4×4 multiplier circuit was performed, and the simulation results were obtained. Modeling of the circuit was performed in QCAD DESIGNER software.*

Index Terms—Quantum-dot cellular automata; majority element; four-bit nano adder; computer edit designed; arithmetic nano circuit.

I. INTRODUCTION

Computer arithmetic plays an important role in information and communication applications such as arithmetic logic unit (ALU) and cryptography. The efficiency of many computer arithmetic applications, first of all, depends on the efficiency of the implementation of the full adder, which is important in computer arithmetic [1] – [3].

The technology of quantum-dot cellular automata (Quantum-dot Cellular Automata, QCA) is a promising technology that can contribute to the further development of Moore's law. In this technology, information is transferred through the formation of a charge instead of a current, which leads to advantages in the circuitry on the spacecraft compared to traditional technologies, such as CMOS technology, in terms of size minimization, speed and energy efficiency [4], [5].

II. ANALYSIS OF RECENT RESEARCH AND PUBLICATIONS

Analyzing past articles [1], [2], we came to the conclusion that the multiplier circuit will have better parameters compared to article [2], if the adder [1] is used.

III. BACKGROUND AND SETTING OF THE TASK

The purpose of the article is to study and consider the main aspects of single-electron multi-bit nanoadders. The main tasks of the article include:

- *Size reduction and power consumption.* One of the main advantages of nanotechnology is the ability to create nanodevices with extremely small dimensions. This allows for reduced power consumption and increased performance, which is important for mobile devices, sensors, medical systems, and more.
- *Quantum computing.* The use of nanotechnology in quantum computing can significantly expand computing capabilities and solve tasks that are beyond the reach of classical computers.
- *Energy efficiency.* The use of ALNP can help reduce energy consumption in electronics, which is an urgent task in connection with the problems of climate change and energy efficiency.

This article aims to increase understanding and awareness of single-electron multi-bit nanoadders and their impact on modern science and technology.

IV. COMPUTER DESIGN NANOCIRCUIT

Considering that the XOR gate is an important gate required to obtain the sum function of a full adder, a better design of the XOR gate is required for the structure of the full adder.

Existing 2- and 3-input XOR logic implementations using QCA are compared in Table I, which suggests that the proposed 3-input XOR logic element is better in terms of cell count, area, and clock phases.

TABLE I. THE COMPARATIVE TABLE FOR REALIZATION GATE 3-XOR

QCA architecture	Number of cells	Area (μm^2)	Delay (number of hours)
Exclusive OR with 2 inputs, design-I	28	0.02	0.75
A 3-input XOR logic element to	14	0.01	0.5
A 3-input XOR logic element to	10	0.01	0.5

In the XOR gate, pulse of sinhronization (clock1) is applied to the inner five quantum cells and npulse (clock0) is applied to the remaining outer cells. The application of the clock to the quantum cells is distinguished by the colors of the cells, as shown in Fig. 1. This three-input XOR gate is used in this tutorial to design a new 1-bit full adder.

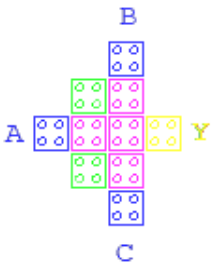

Fig. 1. Three-input XOR gate

In Figure 2a, 1 and 0 indicate the synchronization on the quantum cells, and the arrows indicate the input and output directions. The XOR gate uses a one pulse delay to perform the sum. Pulse 1 will be in the toggle phase when previous pulse 0 is in the hold phase. It takes a quarter of the time period for the device cell data to be in the XOR gate. The MV gate will experience the same delay when processing the execution at the same time as the sum. Thus, the quantum cell pulse in the MV gate must be switched from pulse to pulse in the proposed design, which will generate the execution output with the same delay as the sum output of the XOR gate.

The next important question in the design of quantum cells is how and where the input data is applied. Since the XOR and MV gates have common inputs, the circuit can be implemented as shown in Fig. 2b. If these inputs are applied to each gate separately, more quantum cells are required.

Given where the inputs are located, the inputs input1, input 2, and input 3 can be applied anywhere between the two gates to the cells that exist between them. However, the choice of a quantum cell to supply a particular input depends on the time delay from which the three inputs simultaneously enter the unit cell. The proposed scheme for 3-bit addition of only 26 quantum cells with an area of 0.02 μm^2 is shown in Fig. 2c.

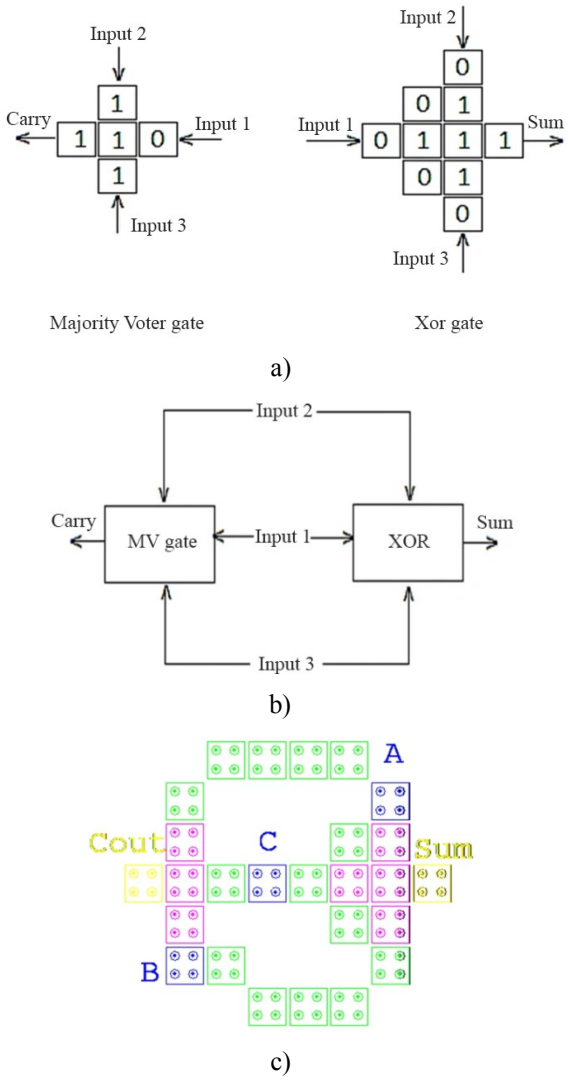

Fig. 2. Block diagram of one bit four adder: (a) is the majority voter element and XOR; (b) is the block-shart; (c) is the QSA proposed circuit

A comparison of the proposed and several existing full adders is shown in Table II to illustrate the improved performance of the proposed full adder design. It can be seen from the table that the proposed design of a 1-bit full adder is much better in both the number of cells and the delay.

Another important parameter to deal with is the energy dissipation of QCA layouts. The energy dissipation of the proposed layout is measured using the QCADesigner-E method using the Coherence Vector Modeling Mechanism setting. A comparison was made with the existing schemes of 1-bit full adder in and, for which the analysis of energy dissipation was carried out. The results of the analysis are given in Table III.

TABLE II. THE COMPARATIVE TABLE OF QCA FOUR ADDER

QCA architecture	Num. of cells	S(μm²)	Delay	Crossover layer
Tougaw and Lent [16]	190	0.2	Without clocking	Coplanar
Angizi adder [13]	95	0.09	1.25	Coplanar
The proposed adder	26	0.02	0.5	Coplanar

TABLE III. TEMPERATURE INDUCTORS OF QCA FOUR ADDERS TABLE

QCA architecture	Sum_Ebath (ev)	Avg_Ebath (eV)	Temperature (K)
Angizi adder [5]	3.52e − 02	3.20e − 03	1
Md. Abdullah-al-shafi adder [12]	2.31e − 02	2.10e − 03	1
The proposed adder	2.23e − 02	2.03e − 03	1

It follows from the table that the proposed adder exhibits the necessary properties at 1 K.

V. OBTAINED RESULTS AND DISCUSSION

The most rational and simple structural diagram of a one-bit adder was created with the help of five-inputs MEs.

The results of the computer design of this nanocircuit using QCADesigner are shown in Figs 3 and 4.

The results of simulation of time characteristics confirm the operability of the five-way majority element.

The functions of adding S and the carry C are determined by the rules for fulfilling the conditions of majority choice [7]:

$$S = \text{maj}\left(x_1, x_0, C_0, \overline{C}\right) = \overline{C}\left(x_1 \vee x_0 \vee C_0\right) \vee x_1 x_0 C_0,$$

$$C = \text{maj}\left(x_1, x_0, C_0\right) = x_1 \vee x_0 \vee x_1 C_0 \vee x_0 C_0.$$

Generalized nanocircuit design results for a one-bit full-adder KA compared to other known one-bit full-adder KSA circuits are given in Table IV.

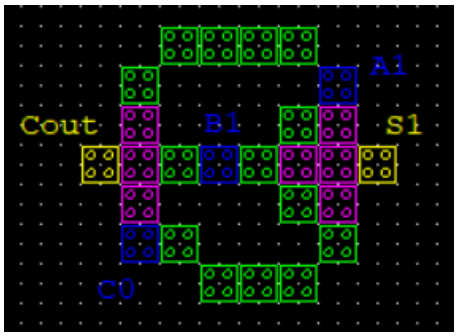

Fig. 3. Project of a complete one-bit adder on a five-inputs ME

Fig. 4. Simulation of the time characteristics of a full one-bit adder on a five-inputs ME

TABLE IV. COMPARISON TABLE FOR ONE-BIT CIRCUITS OF FULL ADDER QCA

Certificate	Number of QA	Area, μm²	Delay, synchronization zones
[9]	71	0.06	5
[10]	52	0.038	4
[14]	63	0.05	3
[16]	46	0.04	4
The result obtained	41	0.07	4

The developed nanocircuit of the four-bit adder is shown on the tablet field of Cade QCADesigner (Fig. 5).

The time diagrams of the operation of the four-bit adder are shown in Fig. 6.

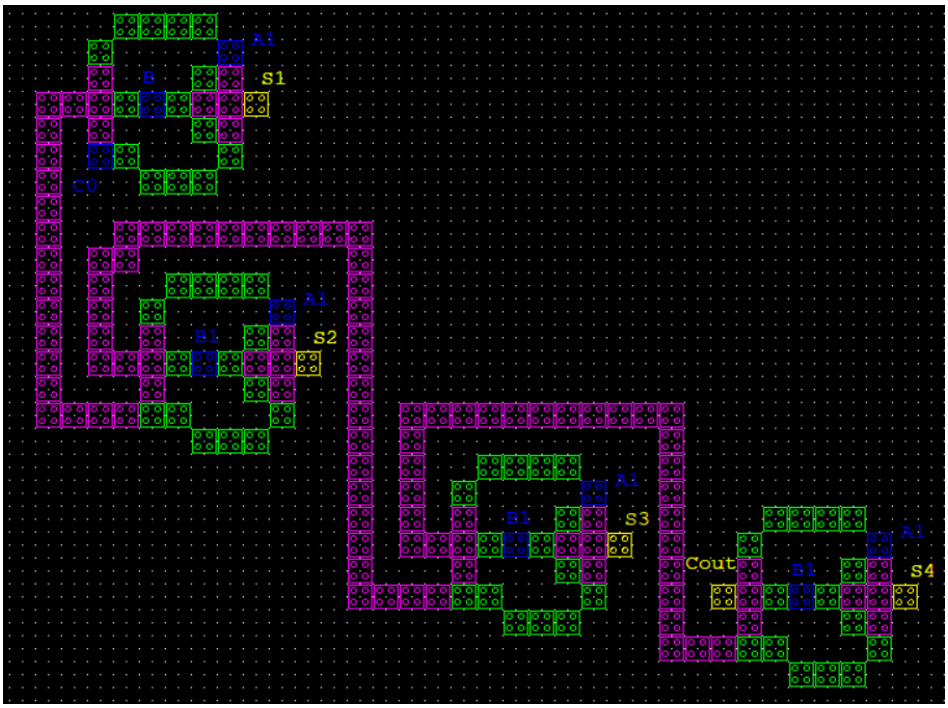

Fig. 5. The result of designing a nanocircuit of a four-bit adder

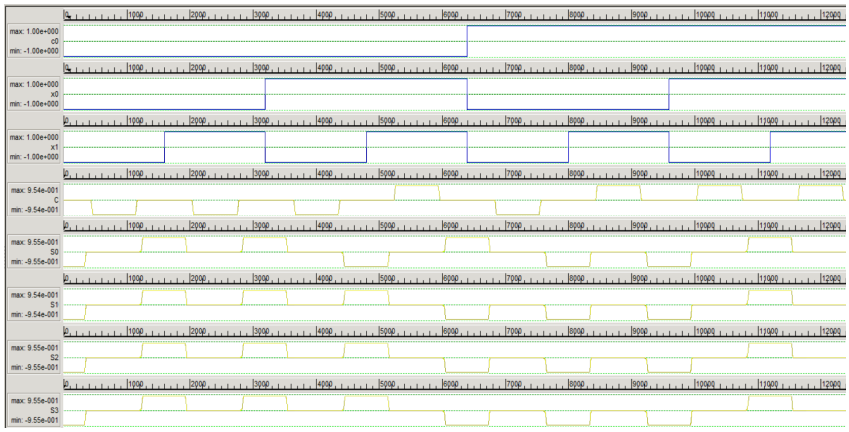

Fig. 6. Results of simulation of time diagrams of a nanocircuit of a four-bit adder

V. CONCLUSIONS

The prospects for the development of arithmetic - logic nanodevices (ALND) are very promising, as they can provide a significant contribution to various fields of science and technology.

Single electron multilevel adders play an important role in arithmetic-logical nanodevices. So, efficient implementation of ALND adders can increase the efficiency of the computer arithmetic circuits. This paper presented and evaluated an efficient full adder circuit in the QCA technology. In addition, we implemented a four-bit QCA nanocircuit based on this new one-bit QCA full adder with majority and XOR gates. The designed circuits have been implemented using the QCADesigner tool version 2.0.3. The implementation results confirmed that the designed circuits outperform recent modified one-bit QCA full adder circuits and four-bit QCA circuits in [5], [13], [16] in terms of complexity, required area and temperature influence.

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О. С. Мельник, М. М. Кравець, В. М. Кравець. Одноелектронні багаторівневі суматори
Оскільки мікроелектронні структури метал-окисел-напівпровідник досягли малорозмірних і квантових обмежень, то в роботі створені технологічні моделі одноелектронних наносхем багаторівневих суматорів.

Доведено, що можна кодувати один біт інформації наявністю або відсутністю одного електрона на квантовому кластері-острівці. У статті представлено моделювання схеми помножувача 4×4 на запропонованому однорозрядному повному суматорі. У результаті проведено порівняння з іншими суматорами, проведено аналіз розсіювання енергії в залежності від температури та розсіюваної потужності існуючих і запропонованих помножувачів у міліваттах. В результаті встановлено, що запропонований суматор має кращі властивості порівняно з аналогічними. В результаті роботи проведено моделювання схеми помножувача 4×4 та отримано результати моделювання. Моделювання схеми виконано в програмі QCAD DESIGNER.
Ключові слова: клітинні автомати з квантовими точками; мажоритарний елемент; чотирирозрядний наносуматор; розроблений комп'ютерний монтаж; арифметична наносхема.

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