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ARITHMETIC-LOGIC SINGLE-ELECTRON NANOCIRCUITS

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Abstract—Computer—added design of single-electron nanoelectronic circuits on quantum majority components has been implemented. Proposed methods of building logic-arithmetic computing devices of the combinational type, which implement an almost complete system of logical functions in both the majority and Boolean bases. Quantum cellular automata is a technology that emerged two decades ago, in which the values of logical states correspond to the positions of individual electrons. Quantum cells are used to construct logic nanoelements and arithmetic nanodevices. The work is dedicated to the computer design of modern logic and arithmetic devices, which include universal majority elements. In the work, quantum nano-devices are modeled using QCADesiner automated design system.

Index Terms—Quantum cellular automata; single-electron tehnology; majority element; computer-aided design; arithmetic-logic devices; nanocircuits.

I. INTRODUCTION

Ouantum cellular automata (OCA) computing paradigm according to which information is represented by a certain configuration of electrons in a cell of quantum automata consisting of one or two separate molecules [1]. The orientation of a pair of quantum cells is such that their mutual arrangement determines the mutual influence. This interaction of charges between neighboring cells makes it possible to process and transmit information. This method is functionally similar to, but structurally different from, the way in which individual gates are combined in large integrated circuits to perform arithmetic-logic operations and create circuits with memory.

II. BASES OF OCA

Devices on QCA consist of nanoscale dielectric cells that have four quantum semiconductor dots located in the corners and two mobile electrons. A separate cell provides tunnel junctions with potential barriers. The transitions are controlled by a local electric field, the magnitude of which increases to hinder the movement of electrons, or decreases to encourage it. Thus, a single cell can be in one of three states. The zero state, or the state of uncertainty, occurs when the potential barrier is reduced, and a mobile electron can occupy any of the vacancies. The other two states, polarization states, occur when the magnitude of the potential barrier increases and maintains its level to minimize the energy level of the cell. The set of states Q is finite and typical: $Q = \{0,1\}$. The probability of a cell being in one of the polarization states can be correlated with the charge density of each individual quantum dot, and is determined by the formula:

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{(\rho_1 + \rho_3) + (\rho_2 + \rho_4)} = \pm 1,$$

where ρ_i is the electric charge density of each quantum dot of the cell.

In Figure 1 shows the single-electron cell of the QCA, two methods of its placement in space and polarization of electrons.

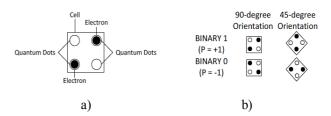


Fig. 1. A cell of a quantum automata (a), its two ways of placement in space (b) and polarization $(P = \pm 1)$

III. LOGICAL MAJORITY ELEMENT AND INVERTER

Placing the cells in sequence one after the other and causing them to interact with each other, it is possible to ensure the flow of information along such a conductor. Theoretically, there are two methods of constructing a conductor depending on the 45-degree or 90-degree orientation of the cells, but it is technologically difficult to produce nanocells with different orientations [3].

With the help of QCA, various elements can be constructed to perform logic and arithmetic operations. The basic logical nanocomponents in the

theory of cellular automata are the majority element (ME) and the inverter (Fig. 2).

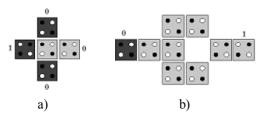


Fig. 2. Three-inputs majority element (a) and inverter (b) based on QCA

The polarization of the ME output cell coincides with the polarizations of most input cells. Boolean expression for the majority function:

$$maj(x_2, x_1, x_0) = x_2x_1 \lor x_2x_0 \lor x_1x_0,$$

where x_2 , x_1 and x_0 input arguments. Fixing the polarization of one of the inputs of the majority element as logical 0 or logical 1 makes it possible to obtain AND or OR elements, respectively $maj(x_2, x_1, 0) = x_2 \cdot x_1$, , $maj(x_2, x_1, 1) = x_2 \vee x_1$. Such cells can be created in the manufacturing process, which eliminates the need to maintain a constant current through the circuit.

IV. ADDERS

Scientists of the Kharkiv University of Radio Electronics [2] and the University of Notre Dame [1] were the first to propose micro- and nano-circuits of

ME-based adders. A one-bit half-adder on the QCA can be composed of four MEs and two inverters (Fig. 3). The expressions for the sum *S* and the carry *C* of this adder are as follows:

$$S = \text{maj}(x\overline{y}, \overline{x}y, 1) = x \oplus y,$$

 $C = \text{maj}(x, y, 0) = xy,$

where x, y are input additions.

In Figure 4 shows the single-electron nanocircuit on the QCA of a one-bit half-adder (a) and the results of modeling its time diagrams on the QCADesiner field [4], [5], [7]. Cells with a 45-degree orientation were used to construct the input conductors. Using this way of placing cells creates an inverting circuit in which each cell is oppositely polarized to the neighboring cells.

If a conductor of equally polarized cells crosses an inverting conductor, the conductors do not interact with each other, so they can work independently at the same level. Such an intersection is called coplanar [3], [6]. The problem of the coplanar crossing is that the distance between the comeasures of a single conductor leads to a decrease in the probability of signal passage. The delay of such an adder is one clock cycle consisting of four clock zones, shown in Fig. 4 different degrees of gray gradation.

A two-bit adder implements arithmetic addition S_2 , S_1 , S_0 two-digit binary numbers x_1x_0 and y_1y_0 is show on Fig. 5.

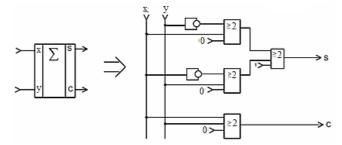


Fig. 3. Circuit of a one-bit half-adder on three-inputs majority elements

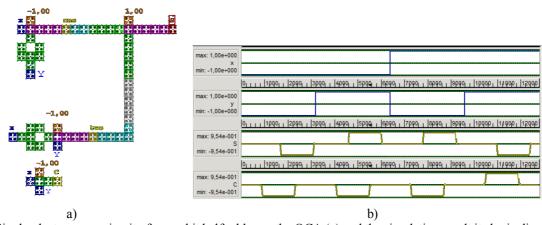


Fig. 4. Single-electron nanocircuit of a one-bit half-adder on the QCA (a) and the simulation result its logic diagrams (b)

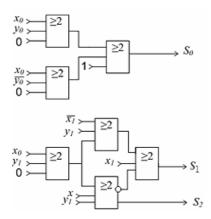
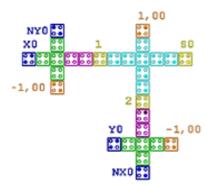


Fig. 5. Nanocircuits of a two-bits adder on two-inputs majority elements

The logic equations for the three outputs of a two-bit adder implemented on seven MEs and one inverter have the form:

$$\begin{split} S_0 &= \mathrm{maj} \big(\mathrm{maj}(x_0, \, \overline{y}_0, 0), \mathrm{maj}(\overline{x}_0, y_0, 0), 1 \big) \\ &= x_0 \overline{y}_0 \vee \overline{x}_0 y_0 = x_0 \oplus y_0, \\ C_0 &= \mathrm{maj}(x_0, y_0, 0) = x_0 y_0, \end{split}$$



$$\begin{split} S_1 &= \mathrm{maj} \Big(\mathrm{maj} (\overline{x_1}, \, y_1, \, C_0), \, x_1, \, \mathrm{maj} (\overline{x_1, y_1, C_0}) \Big) \\ &= \overline{x_1} \overline{y_1} C_0 \vee \overline{x_1} y_1 \overline{C_0} \vee x_1 \overline{y_1} \overline{C_0} \vee x_1 y_1 C_0 \\ &= C_0 \big(\overline{x_1} \overline{y_1} \vee x_1 y_1 \big) \vee \overline{C_0} \big(\overline{x_1} y_1 \vee x_1 \overline{y_1} \big) = (x_1 \oplus y_1) \oplus C_0, \\ S_2 &= \mathrm{maj} \big(C_0, x_1, y_1 \big) = x_1 y_1 \vee x_1 C_0 \vee y_1 C_0. \end{split}$$

Then in Figs 6 and 7 show the results of computer design this nanocircuit using QCAD.

The two-bit adder nanocircuit designed in this way is based on 98 quantum cellular automata, the size of which is (18x18) nm, with four quantum dots with a diameter of 5 nm, the distance between the centers of neighboring cells is 20 nm. The total size of the structure (360x414) nm. There are 11 inputs and three outputs, and four cells have fixed polarization.

When using five-inputs majority elements, we can build the most rational and simple one-bit adder circuit. The structural diagram of a one-bit adder is built on one five-input ME and one three-input (Fig. 8).

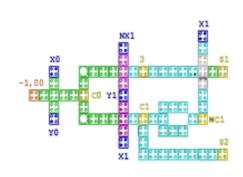


Fig. 6. The project of a two-bit adder nanocircuit

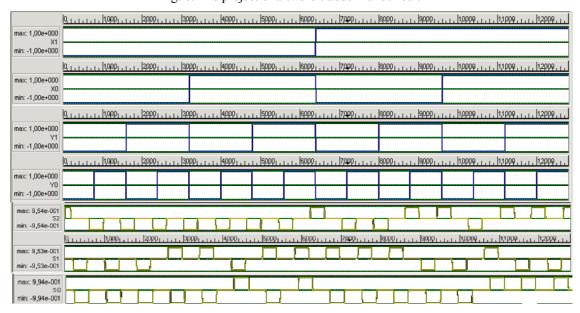


Fig. 7. Modeling the time characteristics of a two-bit adder

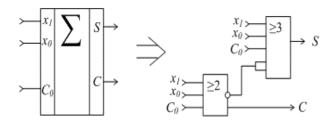


Fig. 8. Circuit of a one-bit adder based on a five-inputs ME

The results of the computer design of this nanocircuit using QCAD are shown in Figs 9 and 10.

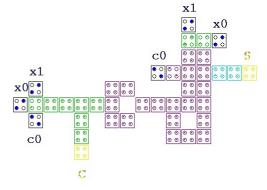


Fig. 9. The project of a full one-bit adder on a five-inputs ME

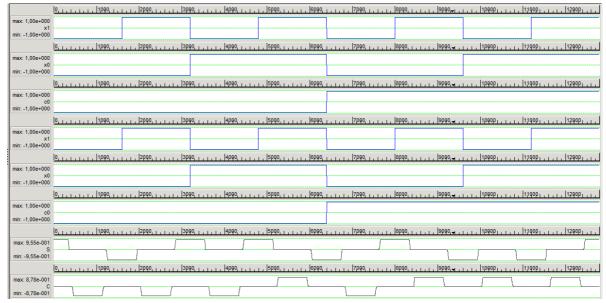


Fig. 10. Modeling the time characteristics of a full one-bit adder on a five-inputs ME

The functions of addition S and carry C are determined by the rules of addition in the majority basis [2]:

$$\begin{split} S &= \mathrm{maj}(x_1, \, x_0, \, C_0, \, \overline{C}) = \overline{C}(x_1 \vee x_0 \vee C_0) \vee x_1 x_0 C_0, \\ C &= \mathrm{maj}(x_1, \, x_0, \, C_0) = x_1 x_0 \vee x_1 C_0 \vee x_0 C_0. \end{split}$$

The simplest full-adder nanocircuit is based on 41 KA, and its total size is (288x162) nm.

V. CONCLUSIONS

Completed computer added design of one- and two-bit single-electron nano-adders. The use of multi-level crossing of conductors avoids the problems of coplanar crossing. The simulation is performed in such a way that the outputs are in the last fourth clock zone, which corresponds to the rest phase after the phase in which the last calculations were performed. Three full clock cycles are required to complete the addition operation. The goal of designing a reliable layering of a two-bit adder nanocircuit and increasing its operational reliability

has been achieved, but the presence of shortcomings and defects associated with the molecular technology of manufacturing quantum cellular automata requires further work in this direction.

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О. С. Мельник, В. О. Козаревич. Арифметико-логічні одноелектронні наносхеми

Реалізовано комп'ютерне проектування одноелектронних наноелектронних схем на квантово-мажоритарних Запропоновано методи побудови логіко-арифметичних компонентах. обчислювальних пристроїв комбінаційного типу, які реалізують практично повну систему логічних функцій як у мажоритарному, так і в булевому базисі. Квантові клітинні автомати – це технологія, яка виникла два десятиліття тому, в якій значення логічних станів відповідають позиціям окремих електронів. Квантові комірки використовуються для побудови логічних наноелементів і арифметичних нанопристроїв. Робота присвячена комп'ютерному проектуванню сучасних логічних і арифметичних пристроїв, які містять універсальні мажоритарні елементи. У роботі квантові нанопристрої моделюються за допомогою автоматизованої системи проектування OCADesiner.

Ключові слова: квантові коміркові автомати; одноелектронні технології; мажоритарний елемент; системи автоматизованого проектування; арифметико-логічні пристрої; наносхеми.

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Напрям наукової діяльності: моделювання пристроїв мікро- та наноелектроніки, автоматизоване проектування, твердотільна електроніка.

Кількість публікацій: більше 170 наукових робіт.

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Напрям наукової діяльності: системи автоматизованого проектування, одноелектронні схеми, твердотільна електроніка.

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