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COMPARATIVE COMPUTER DESIGN OF FOUR-BITS NANOMULTIPLIER

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Abstract*—This paper presents a simulation circuit of a 4x4 Baugh–Wooley multiplier on a proposed one-bit full adder. The results included a comparison with other adders, an analysis of energy dissipation depending on temperature and dissipated power of the existing and proposed multipliers in mW. As a result, it was found that the proposed adder has better properties compared to similar ones. As a result of the work, the simulation circuit of the Baugh–Wooley multiplier 4x4 was performed, and the simulation result was obtained. Computer-edit simulate and design is performed in QCA DESIGNER software.*

Index Terms—Quantum-dots cellular automata; computer- aided design; majority element; multiplier Baugh-Wooley.

I. INTRODUCTION

Scaling of CMOS transistors leads to several problems such as short channel effects, subthreshold conductivity and leakage currents, lithography and fabrication issues [1]. Therefore, it is envisaged that Moore's law cannot be continued for future technologies. Quantum-dot cellular automata (QCA) is a promising transistor-less nanotechnology which is predicted to supplant the current CMOS technology. QCA is a nanotechnology which was proposed in 1993 by C.S. Lent et al. [1]. Later, the first fabrication took place in the year 1997. Quantum cell is the fundamental element of QCA. The quantum cell is square in shape and has four dots arranged at its corners. It also contains two electrons. Due to the electrostatic interactions, these two electrons exhibit two polarizations characterizing the two binary states, logic "0" and logic "1". As a result, all digital circuits can be developed by quantum layouts as shown in [2]. Thus, QCA provide a groundbreaking solution to nanoscale computation, which opens up a new outlook on circuit design.

In any computer arithmetic computation such as addition, subtraction or multiplication, the adder plays a very important role. Consequently, for the design of high-performance arithmetic circuits, an efficient adder is necessary. This paper introduces an energy-efficient and area-optimized 1-bit full adder design in QCA which effectively brings down the number of quantum cells, area and energy dissipation. Further, to demonstrate the efficiency of the proposed full adder design, the Baugh–Wooley multiplication algorithm has been implemented using the proposed 1-bit full adder and its performance has been analyzed in terms of cell count, area, latency and power dissipation.

II. PROPOSED FULL ADDER DESIGN

From the analysis of related works, it can be summed up that current full adder QCA designs have the drawbacks of cell count, area, inefficient clocking and latency. Earlier works [3] – [5] on adders using QCA have primarily focused on reducing majority voter gates. Nonetheless, reducing majority voter gates alone does not reduce the number of cells needed to make the quantum circuit. Therefore, a novel full adder architecture is proposed in this paper, which aims to mitigate the cell count, provide efficient clocking and thereby reduce the circuit latency.

Considering that the XOR gate is the essential gate needed to obtain the sum function of the full adder, a better design of the XOR gate is necessary for a full adder structure. Previous studies that implemented XOR gate have mostly focused on the reduction of majority voter gates. A 3-input XOR gate was designed using explicit cell interaction method in [7], [8], where the data from input cell to device cell propagate with complemented form from all three directions. Two 2-input XOR gate designs using QCA were suggested in [9]. Later in [10], A. N. Bahar et al. proposed a 3-input XOR gate which had fewer cells [6]. This XOR gate was designed with only 10 cells having an area of 0.01 pm2. The existing 2-input and 3-input XOR logic implementations using QCA are compared in Table I

which suggests that the 3-input XOR gate proposed in [10] is better in terms of number of cells, area and clock phases.

TABLE I. COMPARISON OF 3-INPUT XOR GATES

QCA architecture	Number of cells	Area (pm^2)	Delay (no. of clocks)
2-input XOR design-I	28	0.02	0.75
2-input XOR design-II	32	0.04	1
3-input XOR gate in	14	0.02	0.5
3-input XOR gate in	14	0.01	0.5
3-input XOR gate in	10	0.01	0.5

In the XOR gate [10], clock1 is applied to the inner five quantum cells, and clock0 is applied to the remaining outer cells. The application of clocks to the quantum cells is differentiated based on cell colors as shown in Fig. 1. The inputs are applied to clock0 cells, and the output is taken from clock1 cells. The time gap between the two clocks and the arrangement of the cells make the entire logic to work as an XOR function. This 3-input XOR gate [10] is used in this paper to design a novel 1-bit full adder.

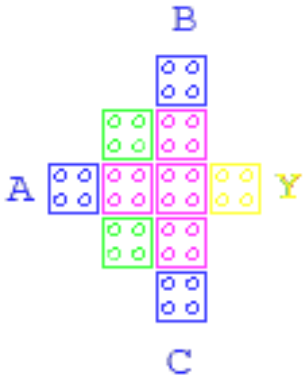


Fig. 1. 3-Input XOR gate [10]

The logic diagram of a 1-bit full adder is shown in Fig. 2.

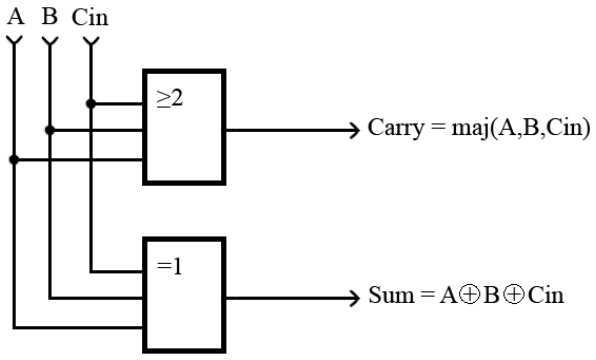


Fig. 2. Logic diagram of a 1-bit full adder circuit

For the 1-bit full adder design proposed in this paper, the 3-input XOR gate [10] is used to obtain the sum output and a majority voter gate for carry output. The novelty can be listed as.

1) Efficient clocking so that there is no delay between sum and carry outputs.

2) 2.Selection of the best possible input application to minimize latency.

3) Reduced cell count.

4) Reduced energy dissipation.

III. COMPARISON OF 1-BIT FULL ADDERS

Comparison of the proposed and several existing full adders is shown in Table II to illustrate the improved performance of the proposed full adder design. Table II gives the total number of cells and the area that the quantum cells occupy in order to build a 1-bit full adder. It is understood from the table that the proposed 1-bit full adder design is much better with regard to both cell number and latency.

TABLE II. COMPARISON OF THE PROPOSED AND SEVERAL EXISTING FULL ADDERS

QCA architecture	No. of cells	Area (pm^2)	Delay	Crossover layer
Tougaw and Lent [2]	190	0.2	Without clocking	Coplanar
Ahmadpour adder [4]	173	0.2	1.25	Coplanar
Roshany adder [11]	25	0.01	0.5	Multilayer
Proposed adder	26	0.02	0.5	Coplanar

III. BAUGH–WOOLEY 4X4 MULTIPLIER DESIGN

The proposed 1-bit full adder is used to build a 4x4 multiplier, which is another important element in DSP processors. A signed multiplication algorithm, proposed by Baugh–Wooley, is implemented here with the proposed full adder. The Baugh-Wooley multiplier equation is as follows:

Consider two signed numbers as

$$A = a_{p-1}2^{p-1} + \sum_{i=0}^{p-2} a_i c^i, \quad B = -b_{p-1}2^{n-1} + \sum_{j=0}^{p-2} b_j c^i,$$

$$P = A \cdot B = \left(-a_{p-1}2^{p-1} + \sum_{i=0}^{p-2} a_i c^i\right)\left(-b_{p-1}2^{n-1} + \sum_{j=0}^{p-2} a_i c^i\right)$$

$$= a_{p-1}b_{p-1}2^{2p-2} + \sum_{i=0}^{p-2}\sum_{j=0}^{p-2} a_i b_i 2^{i+j} - \sum_{j=0}^{p-2} a_{p-1}b_j 2^j 2^{p-1}$$

$$- \sum_{i=0}^{p-2} a_i b_{p-1} 2^i 2^{p-1}$$

complement for the proposed implementation, so that adders can be used for the last two product terms also.

The first negative equation can be solved by taking the product terms as 'ML'

$$M = \sum_{i=0}^{p-2} m_{p-1} 2^{i+p-1}.$$

The addition of bits at positions 22p-1 and 22p-2 is given by:

$$\begin{array}{ccc} & 2^{2p-1} & 2^{2p-2} \\ & 1 & 1 \\ & 1 & 1 \\ 1 & 1 & 0 \end{array}.$$

The additional carry is discarded, and for the 22p−2 bit, 1 is added. At the least bits, the two 1′s are added and a carry is generated which is added in the 2p−1 position. Therefore, the multiplication algorithm can be simplified using the mathematical analysis mentioned above. The terms associated with the negative signs (that is, most significant bits) will have to be complemented.

Figure 3 displays the QCA layout of the 4x4 Baugh-Wooley multiplier designed by means of the proposed full adder. The multiplier is constructed over an area of 1.64 μm^2 with a total of 1638 quantum cells.

Consider the Baugh–Wooley multiplication algorithm for 4x4 multiplication, as shown in Fig. 4.

The proposed full adder is used to add the product terms generated at the intermediate level. As in Fig. 4b, the product terms kept in a box are added by the proposed full adder. The output sum will be taken, and carry will be propagated to the succeeding stages. The last carry generated by the full adder needs to be added to "1". However, instead of addition, the carry bit can be simply complemented using an inverter.

IV. Simulation Results and Discussion

Figure 5 displays the simulation results of the Baugh-Wooley algorithm for different input values. (values are represented in decimal format for understanding).

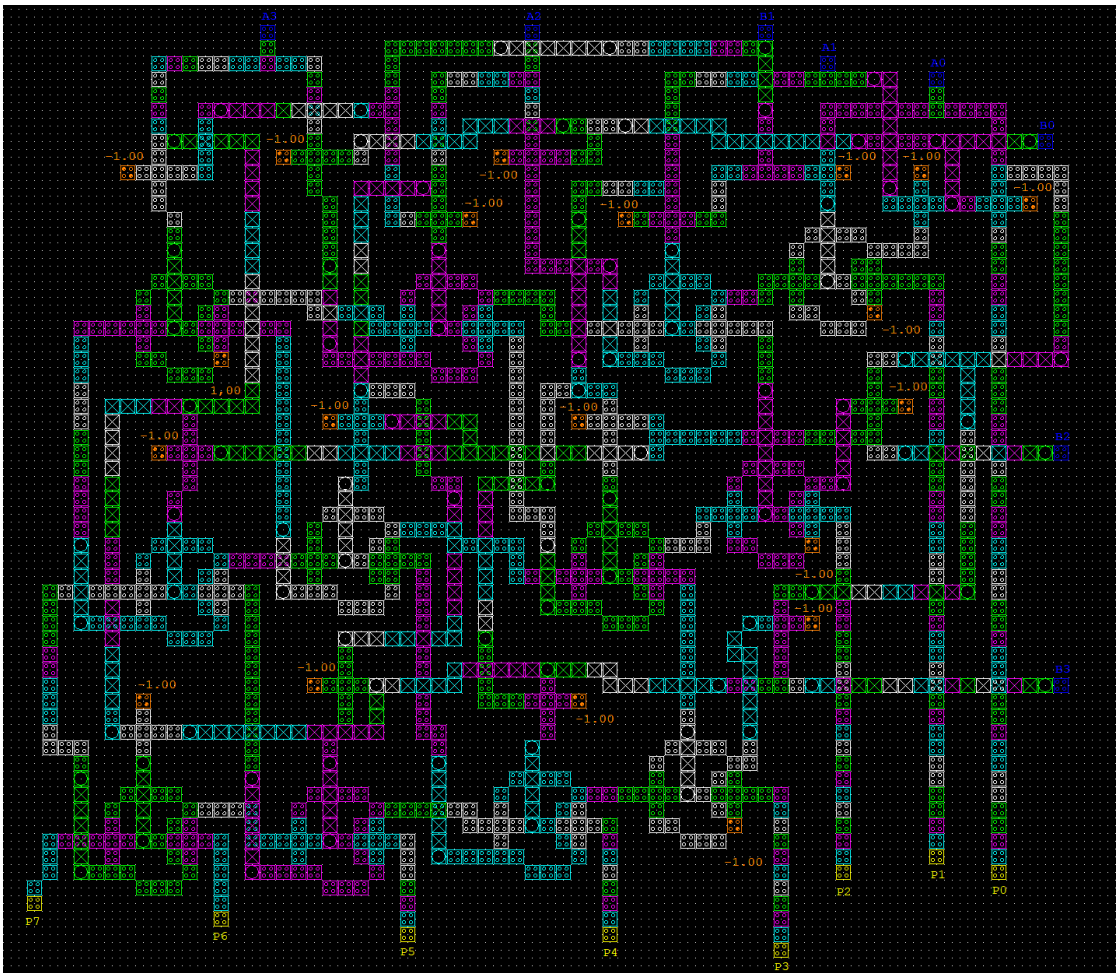
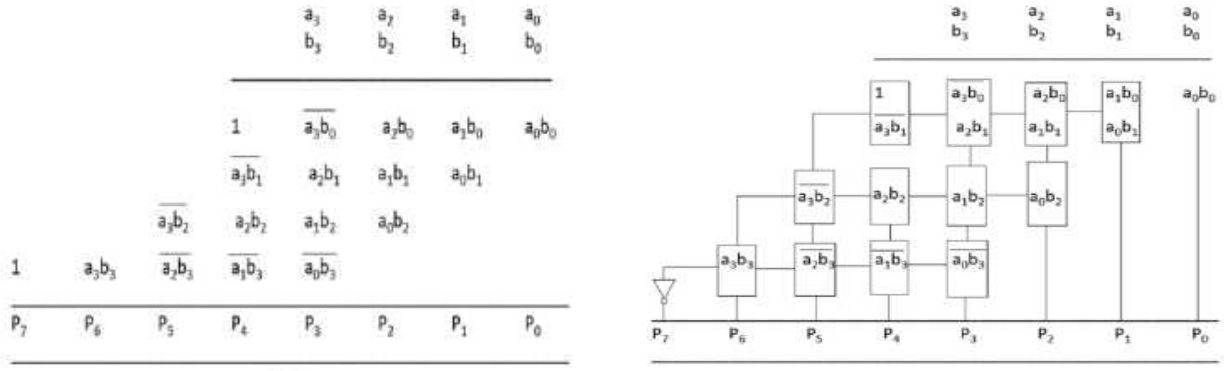


Fig. 3. Layout of proposed 4 × 4 Baugh–Wooley multiplier using the proposed novel full adder design



a) b)

Fig. 4. (a) Baugh-Wooley multiplication and (b) implementation algorithm using the proposed adder [12]

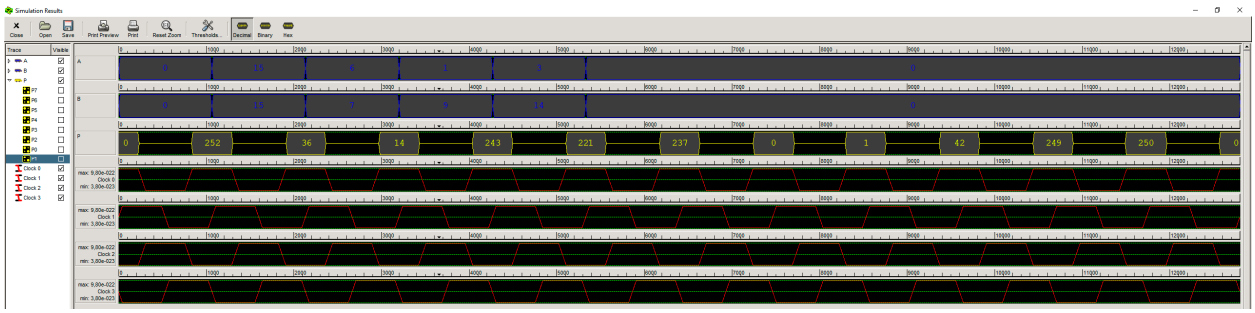


Fig. 5. Simulation results of Baugh-Wooley multiplier implemented using proposed method

Two cases are discussed here:

Case 1

Let A = 0110, B = 0111.

As most bits of the two bits are 0's, there is no requirement to apply 2's complement to both A and B. Multiplication can be applied directly on the two numbers, and it is 00101010. The result in decimal is shown as 42.

Case 2

Consider the numbers to be multiplied as 0001 and 1111, respectively. In decimal, the numbers are 1 and –7, respectively. Since the second number is negative, 2's complement of this is 1001. After multiplying these two numbers, the result will be 10000111 which is shown as –7. (in decimal)

According to the algorithm, the multiplication is as follows:

The result of the algorithm is 249 as shown in Fig. 5 which is in 2's complement. Rewriting in sign magnitude form, the 2's complement of 11111001 = 100000111 = –7.

The simulation results displayed in Fig. 5 indicate that the output is obtained after 6.75 clock pulses. The latency of the result is due to the clock phases used in the quantum cells in the design of the multiplier. Table III [12] presents the cell number, area and propagation delay of the proposed and existing QCA multipliers. As can be seen, compared to the existing design, Baugh-Wooley 4x4 [13], the delay is slightly greater. Nonetheless, the proposed design is efficient, since it reduces the QCA cells by 9% and the area by 17.4%.

Table III. CELL NUMBER, AREA AND PROPAGATION DELAY OF THE PROPOSED AND EXISTING QCA MULTIPLIERS

Method	Cell count	Area (pm^2)	Latency
4x4 serial parallel	264	0.27	0.75
Baugh-Wooley 4x4	1982	1.8	4.75
Proposed Baugh-Wooley 4x4	1638	1.64	6.75

V. CONCLUSION

As quantum-dot cellular automata is one of the potential future nanotechnologies, digital circuits employed in many areas like signal and image processing can be implemented with it. This paper comes up with a novel 1-bit full adder with lesser number of quantum cells in a very small area of 0.02 pm2 with a propagation delay of 0.5 clock cycles. The performance metrics are improved by 8% in the total cells used and with 75% area utilization. The energy dissipation of proposed full adder is also less which is in the order of 2.23e-02 eV at 1 K

temperature, indicating a 4% improvement and 1.01e-02 eV at 38 K temperature, which is 56.7% improvement compared to the existing 1-bit full adder designs. A 4x4 Baugh-Wooley multiplier is implemented using the proposed 1-bit full adder which also demonstrates better performance. The results tabulated prove that the new design requires only 1638 quantum cells within an area of 1.64 pm2. The energy dissipation of the multiplier is just 4.10e-001 eV at 1 K. Unlike the other existing designs, the proposed multiplier circuit is reliable even at 100 K temperature. In addition to this, the power dissipation calculated for 4x4 multiplier design is only 2.44nW.

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О. С. Мельник, М. М. Кравець, В. М. Кравець. Порівняльне комп'ютерне проєктування чотирирозрядного нанопомножувача

У цій роботі представлено схему моделювання множника Боу-Вулі 4x4 на запропонованому однорозрядному повному суматорі. Результати включали порівняння з іншими суматорами, аналіз розсіювання енергії в залежності від температури та розсіюваної потужності існуючих і запропонованих помножувачів у мВт. В результаті встановлено, що запропонований суматор має кращі властивості порівняно з аналогічними. В результаті роботи було виконано моделювання схеми помножувача Боу-Вулі 4x4 та отримано результат моделювання. Комп'ютерне моделювання та проектування виконано в програмному забезпеченні QCA DESIGNER.

Ключові слова—клітинні автомати з квантовими точками; автоматизоване проектування; мажоритарний елемент; множник Боу–Вулі.

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Напрям наукової діяльності: моделювання пристроїв мікро- та наноелектроніки, автоматизоване проектування, твердотільна електроніка.
Кількість публікацій: більше 160 наукових робіт.
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