COMPUTER-AIDED DESIGN SYSTEMS

UDC 621.382.3(045)
DOI:10.18372/1990-5548.61.14218

[1]**O. S. Melnyk,**
[2]**Y. V. Poliakov**

SYNTHESIS OF MAJORITY SINGLE-ELECTRON NANODEVICES WITH MEMORY

[1,2]Faculty of Air Navigation, Electronics & Telecommunications, Nation Aviation University, Kyiv, Ukraine
E-mails: [1]melnyk.olexa@nau.edu.ua ORCID 0000-0003-1072-5526 [2]ibex@ukr.net

Abstract**—***The paper describes the synthesis of reliable sequential nanodevices based on the single-electronics technology of quantum cellular automata. When constructing majority nanocircuits with memory, the theory of finite automata is used. The order of computer design of different types of arithmetic and logic nano-devices is analyzed. Fundamentals of large-logical arithmetic nanocircuit based on multi-narrative selection of unique trigger majority of components on the basis of quantum cellular automata. This creates the preconditions for adaptive implementation of these nanoscales in modern computerized telecommunication systems.*

Index Terms—majority element; sequential nanodevices; quantum automata; one-electronics; computer aided design.

I. INTRODUCTION

There are numerous sources for computer design of sequential micro- and submicron circuits. However, new requirements have emerged for the introduction of modern methods of synthesis of nanoelectronic circuits with memory [1].

In the previous article [2] implemented a spiral loop of memories of nanoregisters on quantum cellular automata (QCA) with control of single inputs. Therefore, the number of internal majoritarian cells can increase by 2n times, where n is the number of controlled inputs. However, with the use of the proposed variants of RC nanotriggers, high-speed read-write (up to 10 ps) is maintained and the nanoscale itself is significantly simplified. The main drawbacks of sources [3], [4] are that the reps of the output of the information takes time to return the synchronized loops to arrive at a nonaddressable address, as well as read the value in the current cell. In article [5], this problem is overcome by parallel transfer and sequential recording in the nanoregister through a multiplex device, which increases the size of the circuit and its energy supply by 20%.

The feature of the successive single-electron nanodevices is the dependence of the output signal not only on current inputs of logical variables, but also on those values of the variables that acted at the inputs at the previous moment of time. To fulfill these conditions, the values of the variables must be remembered by a logical nanodevice. The function of storing values of logical variables in digital nanosets is performed by triggers.

II. PROBLEM STATEMENT

Majority nanodevices with memory differ from majority nanodevices of a combination type of presence of feedback circuits. Such nanodevices are called automata with memory. In Figure 1 shows a generalized circuit of a memory automata.

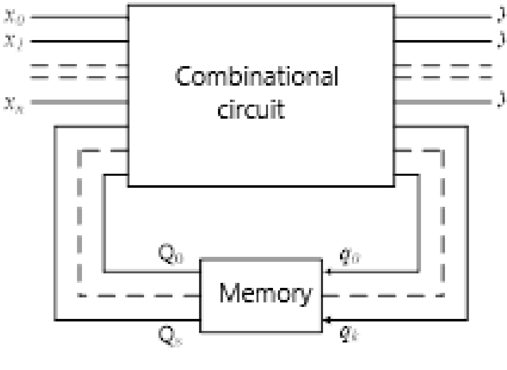


Fig. 1. A generalized circuit of a memory automata

Enter the designation:
$X=(x_0, x_1, ...x_n)$ is the set of input signals;
$Y=(y_0, y_1, ...y_n)$ is the set of output signals;
$q=(q_0, q_1, ...q_n)$ is the set of excitation signals;
$Q=(Q_0, Q_1, ...Q_s)$ is the set of internal states.

Majority nanodevice with memory is given by transitions and outputs functions. The transition function determines the state of the nanoblock at the time (*t* + 1) depending on the state of the nanobody and the values of the input signals at the previous moment of time *t*:

$$Q^{t+1}=\varphi(Q, X)^t. \quad (1)$$

The output function determines the dependence of the output signals of the nanodevice at the time *t* from the state of the nanobody and the values of the input signals at the same time point *t*:

$$Y^t = f(Q,X)^t. \qquad (2)$$

If the output signals are uniquely determined by the states of the nanobody, then there is no need to set the output function. The relations (1) and (2) are executed, based on the conditions of the nanobody. The excitation function is called the dependence of the excitation signal of the elementary automaton on the internal states of all elementary automata of the nanopill device at the time *t* and on the values of the input signals of the node at the same time point *t*:

$$q^t = \eta(Q,X)^t. \qquad (3)$$

The value of the excitation function for a given conversion table is based on the matrix of transitions of the selected elementary automata. The matrix of transitions is called the dependence of the transition of an elementary automaton from its input signals.

III. PROBLEM SOLUTION

Consider the basic principles of constructing and operating the most common trigger nanoelements.

Existing types of flip-flops can be classified according to different features. Most often triggers are classified according to the type of information (setting) inputs used. Distinguish the following types of main trigger information inputs:

R is the separate input trigger reset $(Q=0)$;

S is the separate input of trigger setup $(Q=1)$;

K is the input reset universal trigger $(Q=0)$;

J is the input of the installation of the universal trigger $(Q=1)$;

T is the input trigger entry;

D is the information entry of switching the trigger to a state that corresponds to the logical level at this input;

C is the synchronizing or controlling input.

Thus, the definition of "synchronous *RS*-trigger with inverse static inputs" means that the considered trigger has three information inputs: the input of the set *S*, the input of the reset *R* and the synchronizing input *C*; the switching of the trigger occurs at moments of time due to the appearance of an active logic signal at the input of the synchronization (*C* = 0), and for switching to the inputs *R* or *S* it is necessary to submit a low logical level, that is, a signal logical 0 (*R* = 0 or *S* = 0). Such inputs are respectively designated, $\bar{C}, \bar{R}$ and $\bar{S}$.

Consider the procedure for synthesis basic nanotriggers with different inputs.

The trigger with separate inputs (*RS*-trigger) has an *S* = x_1 input to set to "1" and the input *R* = x_0 to set to "0". Functions of transitions and excitation of a trigger with separate inputs are given in Table I [6], [7].

TABLE I. FUNCTIONS OF TRANSITIONS AND EXCITATION OF THE RS-TRIGGER

x_1	x_0	Q_t	Q_{t+1}	q
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1'	1'	0	–	a_1
1'	1'	1	–	a_2

For prohibited combinations of input signals, noted in Table I units with strokes 1', the excitation function may assume an arbitrary value (a_1, a_2). Depending on the specific values of the uncertain coefficients a_1 and a_2, it is possible to synthesize several variants of only majority nanotrigger in QCA with separate inputs:

1) $a_1 = 1,\ a_2 = 0$:

$$q = \bar{x}_1\bar{x}_0 Q_t \vee x_1\bar{x}_0\bar{Q}_t \vee x_1\bar{x}_0 Q_t \vee x_1\bar{x}_0\bar{Q}_t = x_1\bar{Q}_t \vee \bar{x}_0 Q_t,$$

$$q = \mathrm{maj}(\mathrm{maj}(x_1, \bar{Q}_t, 0),\ \mathrm{maj}(\bar{x}_0, Q_t, 1). \qquad (4)$$

The block diagram and QCA-circuit with majority elements (ME) of single-electron trigger with separate inputs, constructed according to the equation (4), shown in Fig. 2a and b.

2) $a_1 = a_2 = 0$:

$$q = \bar{x}_1\bar{x}_0 Q_t \vee x_1\bar{x}_0\bar{Q}_t \vee x_1\bar{x}_0 Q_t = \bar{x}_0(x_1 \vee Q_t),$$

$$q = \mathrm{maj}(\mathrm{maj}(x_1, Q_t, 1),\ \bar{x}_0, 0). \qquad (5)$$

The second version of the circuit of the trigger with separate inputs according to (5) is shown in Fig. 3.

3) $a_1 = a_2 = 1$:

$$q = \bar{x}_1\bar{x}_0 Q_t \vee x_1\bar{x}_0\bar{Q}_t \vee x_1\bar{x}_0 Q_t \vee x_1 x_0 Q_t = x_1 \vee \bar{x}_0 Q_t,$$

$$q = \mathrm{maj}(\mathrm{maj}(\bar{x}_0, Q_t, 0),\ x_1, 1). \qquad (6)$$

The third variant of the circuit of the trigger with separate inputs (6) is shown in Fig. 4.

4) $a_1 = 0,\ a_2 = 1$:

$$q = \bar{x}_1\bar{x}_0 Q_t \vee x_1\bar{x}_0\bar{Q}_t \vee x_1\bar{x}_0 Q_t \vee x_1 x_0 Q_t$$
$$= x_1\bar{x}_0 \vee \bar{x}_0 Q_t \vee x_1 Q_t).$$
$$q = \mathrm{maj}(\mathrm{maj}(x_1, x_0, x_1),\ \mathrm{maj}(\bar{x}_1, \bar{x}_0, x_1)$$
$$= \mathrm{maj}(x_1, \bar{x}_0, Q_t). \quad (7)$$

The circuit of a trigger with separate inputs, constructed in accordance with equation (7), is shown in Fig. 5.

Thus, a new hierarchical structure of the adaptive selection of trigger nanoscales has been developed according to the criteria a_1 and a_2, decreasing the time of synthesis and computer design, and increasing the speed of all developed nanoregisters to (1) – (7) THz against 100 GHz in existing single-electron prototypes [2] – [5] and decreases power consumption.

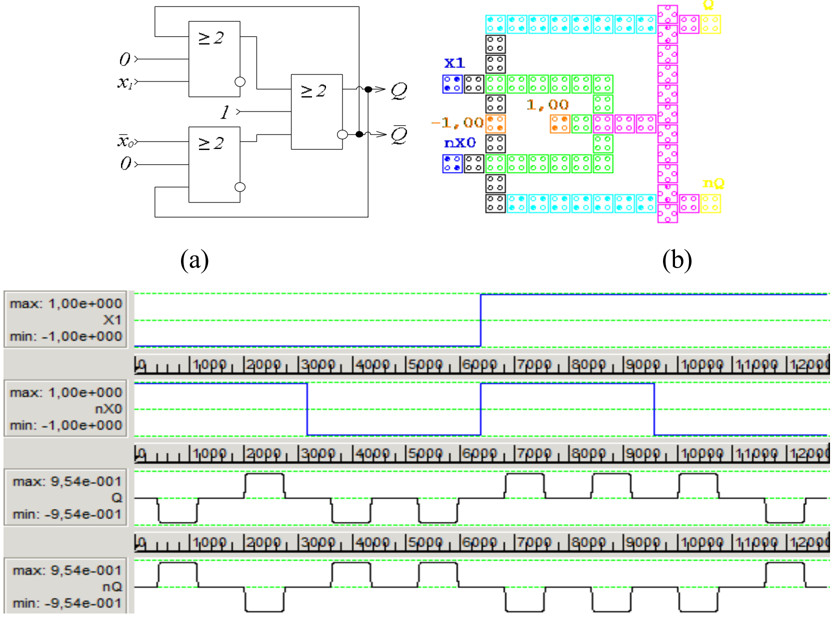
Thus, all four modifications of *RS* nanotraceres to quantum ME have the same time characteristics.

The last version of the *RS*-trigger (Fig. 5) is the most optimal and is implemented only on one universal ME without the use of a constant voltage level [6].

To design single-electron nanoseconders of parallel operation we will use *RS*-triggers with separate inputs. The matrix of transitions of these triggers has the form [7].

Nanoregister of parallel operation without shifting chains, intended for reception and storage of a parallel number code, and is a set of the simplest *RS*-flip-flops with separate inputs (Fig. 5a, b). In Figure 6a circuit and a diagram of a register with control by unit inputs $E = 1$ is shown. In Figure 7a is a register diagram with paraphase inputs. To operate a register with paraphase inputs, it does not need to pre-install it in the state of "0".

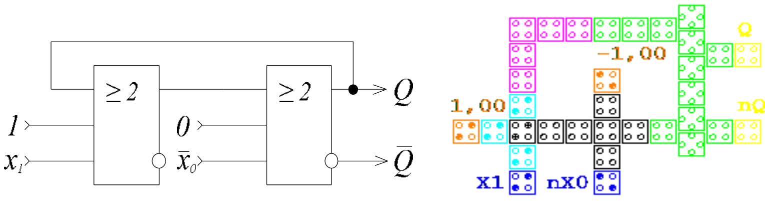
The total number of QCA of the nanoscale register is: 129. Dimensions of QCA: (18×18) nm. The distance between the centers of QCA is 20 nm. Diameters of quantum islands 5 nm. The total dimensions of the register of parallel action are: (340×420) nm.



(a) (b)

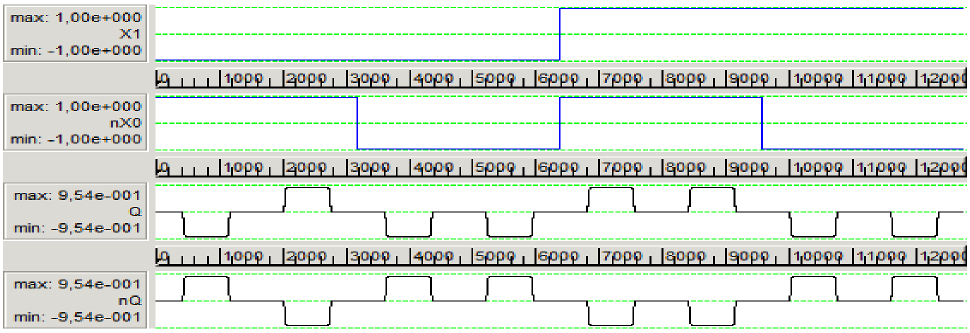
(c)

Fig. 2. Block diagram of *RS*-trigger (modification 1) (a), nanocircuit on QCA (b) and the results of the simulation of the logic states of the *RS*-trigger (c) in CAD QCADesigner [8]



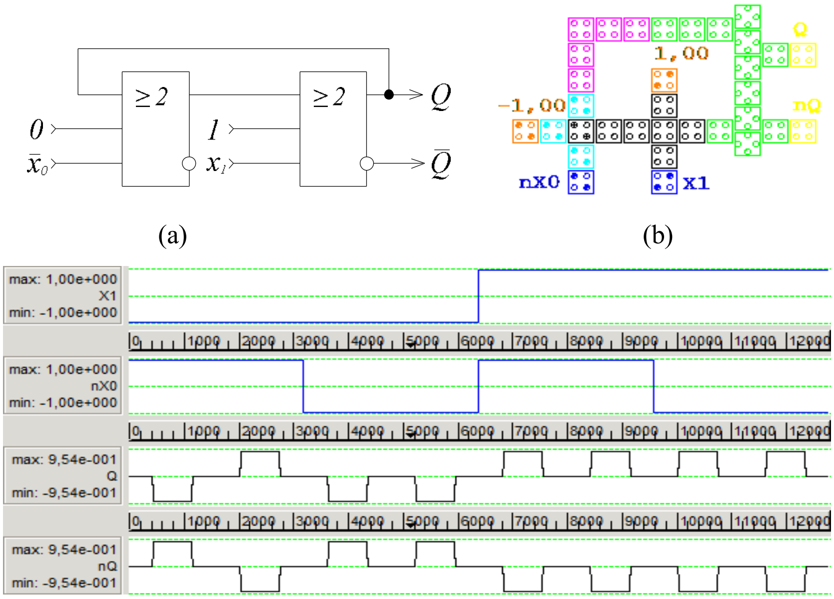
(a) (b)

Fig. 3. Structural circuit of RS-trigger (modification 2) (a), nanoscale on QCA (b) and the results of simulation of waveforms of logic states (c)



(c)

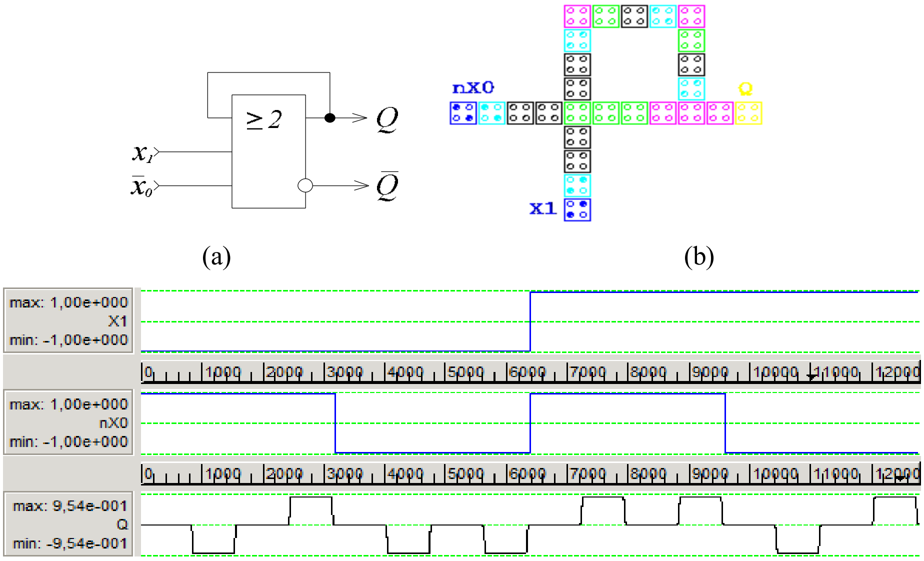
Fig. 3. Ending. (See also p. 38)



(a) (b)

(c)

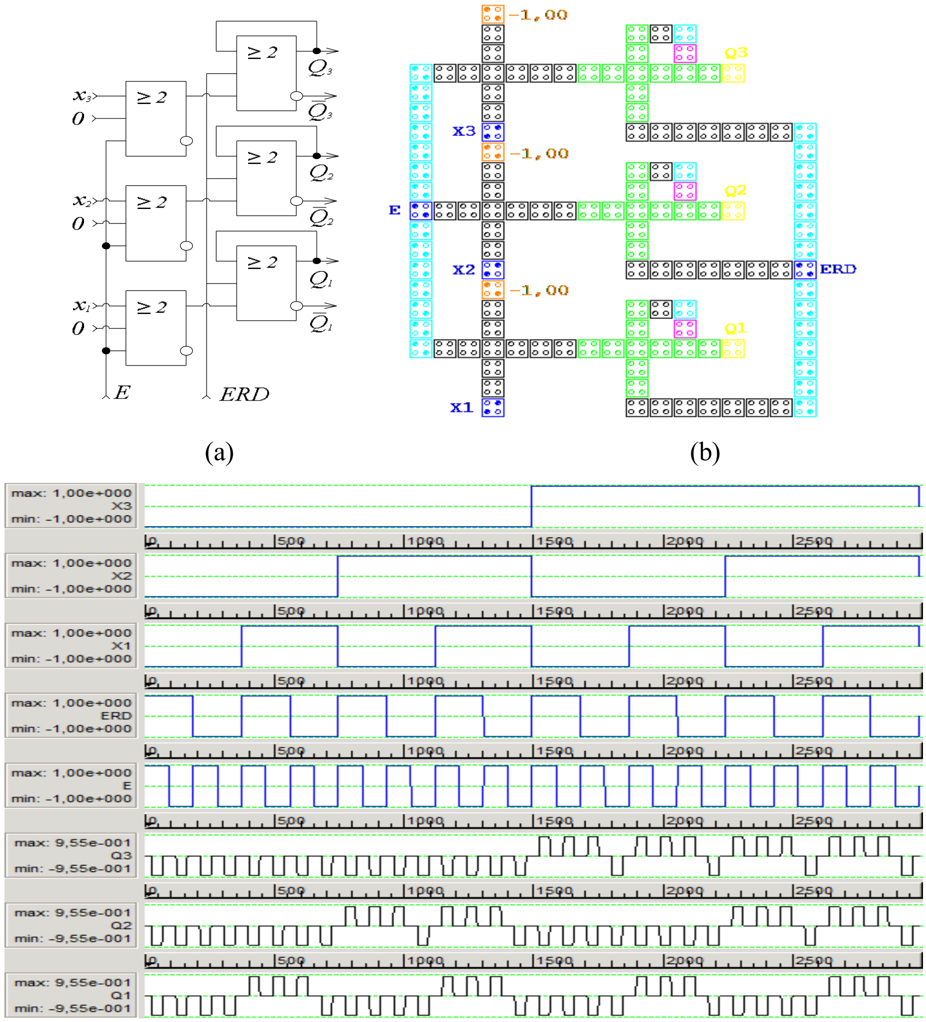
Fig. 4. Structural circuit of RS-trigger (modification 3) (a), nanoscale on QCA (b), and results of simulation of logic states signals in CAD QCADesigner (c)



(a) (b)

(c)

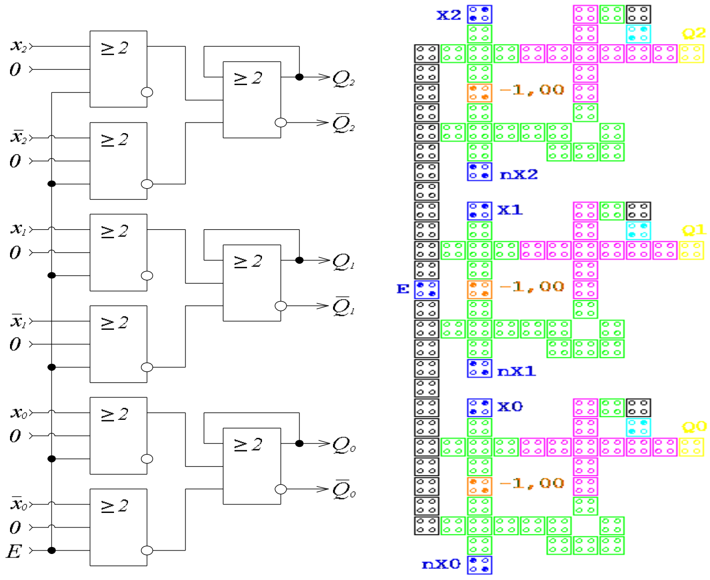
Fig. 5. The block diagram of the RS-trigger (modification 4) (a), the nanoscale on the QCA (b) and results of simulation of signals of logical states (c) in CAD QCADesigner



(a) (b)

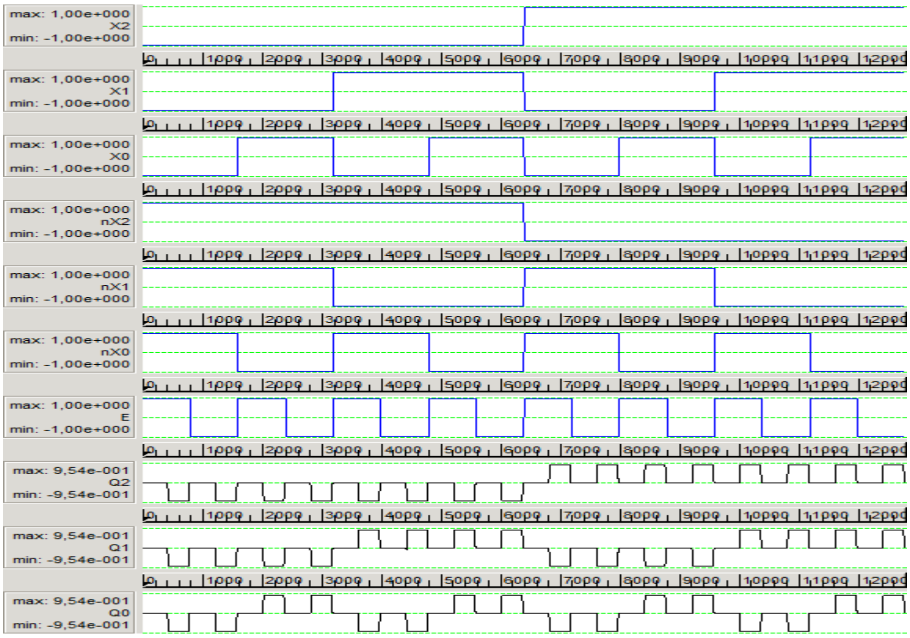
(c)

Fig. 6. Structural circuit of parallel register with control of single inputs (a), nano circuit on QCA (b) and waveforms simulation results (c) in the CAD QCADesigner



(a) (b)

Fig. 7. Structural circuit of paraphase register (a), nanoscale on QCA (b) and results of simulation of waveforms (c) in CAD QCADesigner



(c)

Fig. 7. Ending. (See also p. 40

The total number of QCA of the nanoscale register with paraphase inputs is: 127. Dimensions of QCA: (18×18) nm. The distance between the centers of QCA is 20 nm. Diameters of quantum islands 5 nm. The total size of the register is: (220×580) nm.

IV. CONCLUSION

Because of the clearly defined majoritarian character of the developed circuits of triggers and nanoregisters, each write-reading operation has a minimum number of delay cycles. In previous articles [2]–[5] also used the basic QCA, but the proposed hierarchical organization of CAD information retrieval reduces the design stage and improves the performance characteristics of nanoscale memory.

In the work the computer design of nanodevices of a sequential type with the use of QCADesigner's CAD is implemented. The goal of the nanoscale bundle and their operational reliability has been achieved.

A functionally complete, majority system of nanoelements for the computer design of nanodevices of a sequential type, including nanotriggers with separate inputs and on their basis of nanoregistr, is created.

REFERENCES

[1] C. S. Lent and P. D. Tougaw, "Devices Architecture for Computing whith Quantium Dots," *Proc. of the IEEE,* vol. 10, no. 3, 1997, pp. 73–83.

[2] A. Vetteth, "RAM design using QCA," Proc. of 2013 Nanotechn. Conf. and Trade show, vol. 2, pp. 160–168.

[3] D. Berzon, "A memory design in QCA," Proc. IX-th Symp. At VLST, 2009.

[4] S. Frost, "Memory in motion: study of Storage in QCA," First work. on nonsilicon computing, 2012.

[5] M. Ottavi, "Tile-based design of a serial memory in QCA," Proc. of 15-th ACM Symp. on VLST, April, 2008.

[6] N. I. Pakulov, *The majority principle of building reliable nodes and devices.*: Sov. radio, 1974, 184 p. (in Russian).

[7] O. S. Melnyk and S. O. Todavchych, "Synthesis of Programmable Nanoelectronic Devices," Electronic and Control Systems. no. 4 (32), pp. 89–94, 2013.

[8] K. Walus, "QCA Designer: A Rapid Design and Simulation Tool to QCADII," *Int. Journal of Nanotech and Appl*., no. 1, pp. 1–7, 2005.

Received July 24, 2019

Melnyk Oleksandr. orcid.org/0000-0003-1072-5526. Candidate of Science (Engendering). Associate Professor.
Electronic Department, Faculty of Air Navigation, Electronics & Telecommunications, National Aviation University, Kyiv, Ukraine.
Education: Kyiv Polytechnic Institute, Kyiv, Ukraine, (1971).
Research area: nanoelectronics, computer aid design of nanoelectronic circuits, Simulation of single-electron circuit.
Publications: 155.
E-mail: melnyk.helena@gmail.com

Poliakov Yevhen. Student.
Electronics Department, Faculty of Air Navigation, Electronics & Telecommunications, National Aviation University, Kyiv, Ukraine.
Education: National Aviation University, Kyiv, Ukraine.
Research area: nanoelectronics.
Publications: 12.
E-mail: ibex@ukr.net

О. С. Мельник, Є. В. Поляков. Синтез мажоритарних одноелектронних нанопристроїв з пам'яттю

В роботі описано синтез надійних послідовністних нанопристроїв одноелектроніки на базі технологій квантових коміркових автоматів. Під час побудови мажоритарних наносхем з пам'яттю використовується теорія кінцевих автоматів. Проаналізовано технологію комп'ютерного проектування різних типів послідовністних нанопристроїв. Основа проектування великих логічно-арифметичних наносхем базується на багатоваріативному виборі унікальних тригерних мажоритарних компонентів на базі квантових автоматів. Це створює передумови для адаптивного впровадження цих наносхем у сучасних комп'ютеризованих системах телекомунікацій.

Ключові слова: квантові автомати; мажоритарна логіка; одноелектроніка; нанорегістри.

Мельник Олександр Степанович. orcid.org/0000-0003-1072-5526
Кандидат технічних наук. Доцент.
Кафедра електроніки, Факультет аеронавігації, електроніки та телекомунікацій, Національний авіаційний університет, Київ, Україна.
Освіта: Київський політехнічний інститут, Київ, Україна (1971).
Напрям наукової діяльності: наноелектроніка, автоматизовані системи проектування одноелектронних схем.
Кількість публікацій: 155.
E-mail: melnyk_olexa @gmail.com

Поляков Євген Володимирович. Студент.
Кафедра електроніки, факультет аеронавігації, електроніки та телекомунікацій, Національний авіаційний університет, Київ, Україна.
Освіта: Національний авіаційний університет, Київ, Україна.
Напрям наукової діяльності: наноелектроніка.
Кількість публікацій: 12.
E-mail: ibex@ukr.net

О. С. Мельник, Е. В. Поляков. Синтез мажоритарных одноэлектронных наноустройств с памятью

В работе описан синтез надежных последовательностных наноустройств одноелектроники на базе технологий квантовых ячеистых автоматов. При построении мажоритарных наносхем с памятью используется теория конечных автоматов. Проанализирована технология компьютерного проектирования различных типов последовательностных наноустройств. Основа проектирования больших логически-арифметических наносхем базируются на многовариативном выборе уникальных триггерных мажоритарных компонентов на базе КА. Это создает предпосылки для адаптивного внедрения этих наносхем в современных компьютеризированных системах телекоммуникаций.

Ключевые слова: квантовые автоматы; мажоритарная логика; одноелектроника; нанорегистры.

Мельник Александр Степанович. orcid.org/0000-0003-1072-5526
Кандидат технических наук. Доцент.
Кафедра электроники, Факультет аэронавигации, электроники и телекоммуникаций, Национальный авиационный университет, Киев, Украина.
Образование: Киевский политехнический институт Киев, Украина (1971).
Направление научной деятельности: наноэлектроника, автоматизированные системы проектирования одноэлектронных схем.
Количество публикаций: 155.
E-mail: melnyk_olexa@gmail.com

Поляков Евгений Владимирович. Студент.
Кафедра электроники, факультет аэронавигации, электроники и телекоммуникаций, Национальный авиационный университет, Киев, Украина.
Образование: Национальный авиационный университет, Киев, Украина.
Направление научной деятельности: наноэлектроника.
Количество публикаций: 12.
E-mail: ibex@ukr.net