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ANALYSIS OF THE POTENTIATION DIGITAL-TO-ANALOG CONVERTER WITH ACCOUNTING OF IMPERFECTION ITS BLOCKS

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Abstract*—*Potentiation digital-to-analog converter with iterative additive correction of errors is described. Analysis of errors of this converter with accounting of imperfection its blocks was produced. Basic expressions for the calculation of these errors are listed. The obtained equations conversion and carried out error analysis allow to create high-precision potentiation digital-to-analog converter.

Index Terms—integrator; potentiation digital-to-analog converter; iteratively additive correction of errors; imperfection of blocks; dynamics of the iterative process.

I. INTRODUCTION

It is known that achievement of high linearity transformation functions of information systems related to the collection, processing and transmission of information depends on metrological parameters of the measuring converters used in such information systems, and consequently independence of it's static transformative characteristics from measured value.

Reduction of level of measuring converters error often plays a decisive role in solving the problem of creation of information systems such as automated information-measuring systems, automated control systems, pattern recognition, diagnosis or identification.

II. PROBLEM STATEMENT

In work [1] the measuring converter offered by the author [2], [3] has been considered. It is an iteratively integrating code-voltage converter with additive correction of errors.

If to speak about this measuring converter from the point of view of his function of transformation, then it is the DAC, in which the output voltage is directly proportional to the input code given in decibels.

In work [1] are considered the equation of transformation and the main equations for definition of errors of this measuring converter without accounting of imperfection of it's components (blocks).

However, in the course of design of the measuring converter it isn't enough. In this case we need to have the main equations with taking into account of not ideality of components of the considered measuring converter.

Derivation of such equations is the main objective of this work.

III. MAIN EQUATIONS WITHOUT TAKING INTO ACCOUNT OF IMPERFECTION OF BLOCKS

The structural scheme of iteratively integrating code-voltage converter with additive correction of errors is shown in Fig. 1.

Here I is integrator; SH is sample-and-hold device; SW1 and SW2 are analog keys; RFG is reference frequency generator; CC1 and CC2 are code converters; CTIC1 and CTIC2 are converters of code into the time intervals; STI is shaper of time intervals; E_0 is reference voltage; $N = \lambda + \mu$ are the input code; U_{out} is output voltage; OC is output converter, BC is back converter.

For convenience the equation of transformation and the main equations for definition of errors of this measuring converter without not ideality of his components are given below.

Nonlinearity which is realized in the converter corresponds to the operation of potentiation, i.e. function which is inverse to obtaining logarithm. The input code is given in decibels (dB).

Output voltage value relative to a value of U_0, corresponding to input code $N = 0$ dB:

$$N\,(\text{dB}) = 20 \lg U_{out} / U_0.$$

Equation of converting of this potentiation converter:

$$U_{out} = U_0 10^{N/20}.$$

If the submit an input code N as the sum of two terms (for example, integers and tenths) $N = \lambda + \mu$, conversion equation can be transformed to:

$$U_{out} = U_0 10^{\lambda/20} / 10^{-\mu/20}.$$

After the ending of the first and second conversion cycles the output voltage U_{out} is equal to:

$$U_1 = (E_0 \lambda K_\lambda K_{SH} K_{RP} K_A / f_0 RC) - U_0 Q_H$$

and

$$U_2 = (E_0 \lambda K_\lambda K_{SH} K_{RP} K_A / f_0 RC)(1 - Q_H) - U_0 Q_H,$$

respectively, where: K_λ , K_μ, K_{SH} and K_{RP} , K_A , K_{VD} – are transfer coefficients of the devices CC1, CC2,

SH, OC and BC respectively, f_0 is reference frequency; R and C resistance and capacitance of integrator's resistor and capacitor respectively; and

$$Q_{\text{H}} = 1 - \mu K_{\mu} K_{\text{SH}} K_{\text{RP}} K_{\text{A}} K_{\text{VD}} / f_0 RC.$$

Output voltage of the code-voltage converter after the end of nth cycle; $j = \overline{1,n}$:

$$U_n = (E_0 \lambda K_{\lambda} K_{\text{SH}} K_{\text{RP}} K_{\text{A}} / f_0 RC) \sum_{\text{j}=1}^{n} Q_{\text{H}}^{\text{j}-1} - U_0 Q_{\text{H}}^n$$

$$= \frac{E_0 \lambda K_{\lambda}}{\mu K_{\mu} K_{\text{VD}}} (1 - Q_{\text{H}}) - U_0 Q_{\text{H}}^n = U_{\infty} - \Delta U Q_{\text{H}}^n.$$

where U_n is output voltage of the code-voltage converter after the end of nth cycle; $j = \overline{1,n}$.

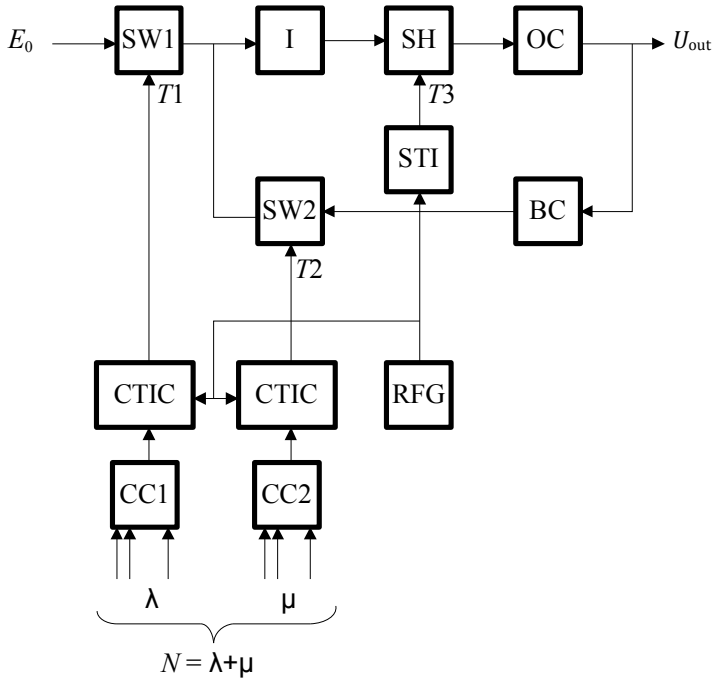

Fig. 1. Potentiation digital-to-analog converter

If the condition $|Q_{\text{H}}| < 0$ is fulfilled, output voltage of the potentiation digital-to-analog converter at the steady-state condition ($n \to \infty$) is determined by the expression

$$U_{\infty} = \frac{E_0 \lambda K_{\lambda}}{\mu K_{\mu} K_{\text{VD}}} = \frac{E_0}{K_{\text{VD}}} 10^{(\lambda+\mu)/20},$$

where

$$K_{\lambda} = \frac{10^{\lambda/20}}{\lambda}, \qquad K_{\mu} = \frac{10^{-\mu/20}}{\mu}.$$

The relative error of conversion γ_n:

$$\gamma_n = \frac{U_n - U_{\infty}}{U_{\infty}} = \frac{\Delta U Q_{\text{H}}^n}{U_{\infty}},$$

where $\Delta U = U_{\infty} - U_0$.

Number of cycles n, corresponding to this error γ_n:

$$n = \left\lceil \frac{\ln \left| \frac{\gamma_n U_{\infty}}{\Delta U} \right|}{\ln |Q_{\text{H}}|} \right\rceil + 1.$$

Basic expressions for the iteratively integrating code-voltage converter with additive correction of errors with taking into account of imperfection it's blocks are summarized in Table 1 – 3 (details of the derivation of these expressions, as well as others discussed below, can be found in work [2]).

IV. Equations with Taking into Account of Imperfection of Integrator's Static Parameters and of Imperfection of Back Converter

To take into account the effect of the additive and multiplicative errors ΔE_0, Δ_I, Δ_{VD}, γ_E, γ_{VD}, respectively, reference voltage source E_0, an integrator I and a back converter BC, the error of the time intervals $T1$ and $T2$ formation and it's jitter, we use the results obtained in [1], expressions, denoting,

respectively, through $\delta T1$, $\delta T2$, $\delta\tau_{\text{Up1}}$, $\delta\tau_{\text{Dn1}}$, $\delta\tau_{\text{Up2}}$, $\delta\tau_{\text{Dn2}}$ the relative errors of interval $T1$ and $T2$ formation, and relative increment of duration of the rise and fall of current through the SW1 and SW2 keys.

Curves rise and fall times of the currents flowing through the SW1 and SW2 keys when switching we approximate by straight line segments. Whereby the effective time from the point of view of forming volt-second area for $T1$ and $T2$, respectively, equal to

$$T1' = T1 - \frac{\tau_{\text{Up1}} - \tau_{\text{Dn1}}}{2}, \quad T2' = T2 - \frac{\tau_{\text{Up2}} - \tau_{\text{Dn2}}}{2},$$

where τ_{Up1}, τ_{Dn1}, τ_{Up2} and τ_{Dn2} are rise and fall times of the currents flowing through the SW1 and SW2 keys when switching with the approximation, respectively.

The expressions obtained for determining the output voltage in the steady state $U_{\infty\text{M}}$ and $U_{\infty\text{A}}$ with the multiplicative and additive errors, respectively, and the corresponding relative errors γ_{STM} and γ_{STA} are shown below, where Δ_I and Δ_{VD} are additive errors of the integrator I and the back converter BC given to the inputs of the respective blocks.

$$U_{\infty\text{M}} = \frac{E_0 T1(1+\gamma_E)}{K_{\text{VD}} T2(1+\gamma_{\text{VD}})}$$

$$\approx \frac{E_0 T1}{K_{\text{VD}} T2}(1+\gamma_E-\gamma_{\text{VD}}) = \frac{E_0 T1}{K_{\text{VD}} T2}(1+\gamma_E-\gamma_{\text{VD}}),$$

$$\gamma_{\text{STM}} = \frac{U_{\infty\text{M}} - U_\infty}{U_\infty} = \gamma_E - \gamma_{\text{VD}},$$

$$U_{\infty\text{A}} = U_\infty\left(1+\gamma_{T1}-\gamma_{T2}+\frac{\Delta E_0}{E_0}+\frac{T_C\Delta_I}{E_0 T1}+\frac{\Delta_{\text{VD}}}{U_\infty}\right),$$

$$\gamma_{\text{STA}} = -\gamma_{T1}+\gamma_{T2}-\frac{\Delta E_0}{E_0}-\frac{T_C\Delta_I}{E_0 T1}-\frac{\Delta_{\text{VD}}}{U_\infty},$$

where

$$\gamma_{T1} = \frac{T1\delta T1}{T1-\frac{\tau_{\text{Up1}}-\tau_{\text{Dn1}}}{2}} + \frac{\frac{\tau_{\text{Up1}}}{2}\delta\tau_{\text{Up1}} - \frac{\tau_{\text{Dn1}}}{2}\delta\tau_{\text{Dn1}}}{T1-\frac{\tau_{\text{Up1}}-\tau_{\text{Dn1}}}{2}} \approx \delta T1 + \frac{\tau_{\text{Up1}}\delta\tau_{\text{Up1}} - \tau_{\text{Dn1}}\delta\tau_{\text{Dn1}}}{2T1},$$

$$\gamma_{T2} = \frac{T2\delta T2}{T2-\frac{\tau_{\text{Up2}}-\tau_{\text{Dn2}}}{2}} + \frac{\frac{\tau_{\text{Up2}}}{2}\delta\tau_{\text{Up2}} - \frac{\tau_{\text{Dn2}}}{2}\delta\tau_{\text{Dn2}}}{T2-\frac{\tau_{\text{Up2}}-\tau_{\text{Dn2}}}{2}} \approx \delta T2 + \frac{\tau_{\text{Up2}}\delta\tau_{\text{Up2}} - \tau_{\text{Dn2}}\delta\tau_{\text{Dn2}}}{2T2}.$$

V. Equations with Taking into Account of Imperfection of Analog Keys

To take into account of imperfection of keys lets denote resistance of the opened keys SW1 and SW2 as $R_{1\text{O}}$ and $R_{2\text{O}}$, and resistance of the closed keys as $R_{1\text{C}}$ and $R_{2\text{C}}$, respectively.

Equations for determining the output voltage in the steady state $U_{\infty\text{Rl}}$, the relative errors of output voltage in the nth cycle $\gamma_{n\text{Rl}}$ and in the steady state $\gamma_{\text{St Rl}}$ in view of these resistances of keys SW1 and SW2 [5], [6] are shown below.

$$U_{\infty\text{Rl}} = \frac{E_0\left(\frac{\lambda K_\lambda}{R+R_{1\text{O}}}+\frac{\mu K_\mu}{R+R_{1\text{C}}}\right)}{K_{\text{VD}}\left(\frac{\mu K_\mu}{R+R_{2\text{O}}}+\frac{\lambda K_\lambda}{R+R_{2\text{C}}}\right)}$$

$$\gamma_{n\text{Rl}} = \frac{U_{n\text{Rl}} - U_{\infty\text{Rl}}}{U_{\infty\text{Rl}}} = \frac{\Delta U_{\text{Rl}} Q_{\text{HRl}}^n}{U_{\infty\text{Rl}}}$$

$$\gamma_{\text{St Rl}} = \frac{U_{\infty\text{Rl}} - U_\infty}{U_{\infty\text{Rl}}} = \frac{\mu K_\mu\left(\frac{\lambda K_\lambda}{R+R_{1\text{O}}}+\frac{\mu K_\mu}{R+R_{1\text{C}}}\right)}{\lambda K_\lambda\left(\frac{\mu K_\mu}{R+R_{2\text{O}}}+\frac{\lambda K_\lambda}{R+R_{2\text{C}}}\right)},$$

where

$$Q_{\text{HRl}} = 1 - \frac{K_{\text{SH}} K_{\text{RP}} K_{\text{A}} K_{\text{VD}}}{Cf_0}\left(\frac{\mu K_\mu}{R+R_{2\text{O}}}+\frac{\lambda K_\lambda}{R+R_{2\text{C}}}\right),$$

$$\Delta U_{\text{Rl}} = U_{\infty\text{Rl}} - U_\infty.$$

VI. Conclusion

Potentiation digital-to-analog converter, i.e. DAC, in which the output voltage is directly proportional to the input code given in decibels, based on iteratively integrating code-voltage converter with iterative additive correction of errors, is considered. Analysis of errors of this converter with accounting of imperfection its blocks was produced. Test results and operation experience confirmed the correctness

of the results of theoretical research. Basic expressions for the calculation of these errors are listed and it allow you to create such high-precision potentiation digital-to-analog converter.

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І. Ю. Сергеєв. Аналіз потенціюючого цифро-аналогового перетворювача з урахуванням неідеальностіості його блоків

Розглянуто потенціюючий цифро-аналоговий перетворювач з ітераційною адитивною корекцією похибок. Виконано аналіз похибок цього перетворювача з урахуванням неідеальності його блоків. Отримані рівняння перетворення та проведений аналіз похибок дозволять створити високоточний потенціюючий цифро-аналоговий перетворювач.

Ключові слова: інтегратор; потенціюючий цифро-аналоговий перетворювач; ітераційна адитивна корекція похибок; неідеальність блоків; динаміка ітераційного процесу.

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И. Ю. Сергеев. Анализ потенцирующего цифро-аналогового преобразователя с учетом неидеальности его блоков

Рассмотрен потенцирующий цифро-аналоговый преобразователь с итерационной аддитивной коррекцией погрешности. Выполнен анализ погрешностей этого преобразователя с учетом неидеальности его блоков. Полученные уравнение преобразования и проведенный анализ погрешностей позволят создать высокоточный потенцирующий цифро-аналоговый преобразователь.

Ключевые слова: интегратор; потенцирующий цифро-аналоговый преобразователь; итерационная аддитивная коррекция погрешностей; неидеальность блоков; динамика итерационного процесса.

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