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# PROGRAMMABLES NANOELECTRONICS GATES

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**Abstract.** *This paper presents a quantum dot cellular automata programmable nanoelectronics gate composed from simple three majority gates. This 7-input gate can be configured into many useful gate structures such as a 4-input AND gate, a 4-input OR gate, a product of sums representation, a sum of products representation, and its variations.*

**Keywords:** quantum cellular automata; majority gate; programmable nanoelectronics gate.

## I. INTRODUCTION

Physical limitations foreshadow the eventual end to a traditional CMOS scaling. Therefore, interest has turned to various nanotechnologies vying to succeed traditional CMOS. Quantum dot cellular automata (QCA), first described in [1], is one of these technologies. The fundamental logic structure for QCA is a majority gate [2]. It has been shown that these gates can be used to form more familiar gates implementing one functions such as AND and OR. This paper considers the computer-aided design of programmable nanoelectronics gates (PNEG) having sevent inputs and three outputs for these majority gates [3], [4].

## II. BACKGROUND OF QCA THEORY

Quantum dot cellular automata provides a very different computation platform than traditional CMOS, one in which polarization, rather than current, contains the digital information and one in which the cells themselves, rather than interconnecting wires. transmit this information throughout the circuit. This section begins with a brief overview of QCA cells and the wires that are composed of QCA cells. This is followed by a description of the QCA majority gate and the various structures PNEG that can be formed by reconfiguring this basic gate.

Quantum dot cellular automata cells are described in [1], [3] as shown in Fig. l, these cells are dielectric square rectangles containing a semiconductor quantum dot in each corner. Two extra electrons, present within each cell, can tunnel from dot to dot within a cell, however they are unable to travel beyond the cell boundaries to neighboring cells. The two degenerate polarizations formed by these electrons are used to represent a logic value of “0” and a logic value of “1” as shown on the left and on the right of Fig. l respectively.

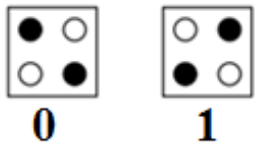



Fig. 1. Quantum dot cellular automata polarizations cells

The QCA cells themselves comprise the interconnecting wires, an example of a QCA wire is shown in Fig. 2. In this example, a value of 1 is transmitted along the wire. Only a slight polarization in a cell is required to fully polarize its neighbor. The direction for the flow of information through a gate or a wire is controlled by a four stage clocking system which raises and lowers barriers between the cells.

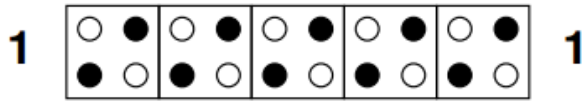



Fig. 2. Quantum dot cellular automata wire

The fundamental logic gate for QCA is the majority gate shown in Fig. 3 that is composed of five cells. Three of these, representing the inputs to the cell, are labeled $x_2$, $x_1$ and $x_0$. The central cell is the major cell that performs the calculation. The remaining cell, labeled $f$, provides the output.

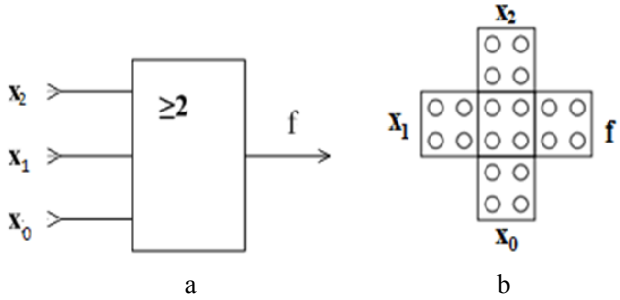
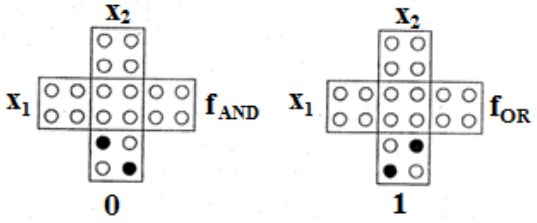



Fig. 3. Majority gate: graphical symbol (a) and QCA realization (b)

The circuit shown in Fig. 3 performs the majority and Boolean function:

$$f = maj(x_2, x_1, x_0) = x_2x_1 \vee x_2x_0 \vee x_1x_0. \quad (1)$$

The other Boolean logic gates formed by programming the polarization of one input $x_0$ to the majority gate to be a constant value. Fig. 4 illustrates a 2-AND gate (a) and a 2-OR gate (b) formed in this manner.




a b

Fig. 4. 2-AND (a) and 2-OR (b) gates

By replacing input $x_0$ with a cell having a fixed polarization of "0", the majority gate functions as an 2-AND gate. In the example 2-AND gate on Fig. 4a have from equation (1) reduced:

$$f_{AND} = maj(x_2x_1x_0) = x_2x_1.$$

Similarly, replacing input $x_0$ with a cell having a fixed polarization of 1 creates a 2-OR gate. In the example 2-OR gate on Fig. 4b:

$$f_{OR} = maj(x_2x_1x_0) = x_2 \vee x_1.$$

Despite that the fundamental logic structure of QCA is the majority gate, many of the attempts to implement functional circuits using these majority gates begin by restricting them to a subset of their full information content potential. Previous complex gates, requiring more than one device cell are described in the literature, however these complex gates are still restricted to implementing several input functions. In [2], a complex gate is used to implement a 2-XOR function. In [4], a majority gate restricted to an 2-AND gate configuration followed by an inverter was used to form 2-NAND building blocks for an field programmable gates array (FPGA) implementation. An alternative to this approach however, is to use the majority gate as a building block to build even larger and more complex PNEG containing multiple programmable and information inputs, and some information outputs.

## III. PROGRAMMABLE NANOELECTRONICS GATES

Fig. 5 shows a 7-input and 3-outputs PNEG. This gate is composed of three majority gates. Three of the inputs to this gate $p_2$, $p_1$ and $p_0$, function as programmables inputs that are used to specify the functionality of the circuit. The remain four inputs. $x_3, x_2, x_1$ and $x_0$, are used to implement Boolean functions of two or four variables. The functionality of this gate for all configurations has been computer-aided designed using QCADesigner [5].

At output of its PNEG formed three main functions which described in majority and Boolean bases:

$$f_1 = maj(x_3, x_2, p_2) = x_3x_2 \vee x_3p_2 \vee x_2p_2, \quad (2)$$

$$f_2 = maj\left[maj(x_3, x_2, p_2), maj(x_1, x_0, p_0)\right]$$
$$= (x_3x_2 \vee x_3p_2 \vee x_2p_2)p_1 \vee (x_3x_2 \vee x_3p_2 \vee x_2p_2) \quad (3)$$
$$\times (x_1x_0 \vee x_1p_0 \vee x_0p_0) \vee p_1(x_1x_0 \vee x_1p_0 \vee x_0p_0).$$

$$f_3 = maj(x_1, x_0, p_0) = (x_1x_0 \vee x_1p_0 \vee x_0p_0). \quad (4)$$

Table 1 provide the resulting Boolean functions (2), (3) and (4) if inputs $p_2, p_1$ and $p_0$ are selected as the three programmables inputs to the PNEG.

TABLE 1

**Programmable inputs and correponding output functions of two or four arguments**

| $p_2$ | $p_1$ | $p_0$ | $f_1(x_3x_2)$ | $f_2(x_3,x_2,x_1,x_0)$ | $f_3(x_1,x_0)$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | $x_3x_2$ | $x_3x_2x_1x_0$ | $x_1x_0$ |
| 0 | 0 | 1 | | $x_3x_2(x_1 \vee x_0)$ | $x_1 \vee x_0$ |
| 0 | 1 | 0 | | $x_3x_2 \vee x_1x_0$ | $x_1x_0$ |
| 0 | 1 | 1 | | $x_3x_2 \vee (x_1 \vee x_0)$ | $x_1 \vee x_0$ |
| 1 | 0 | 0 | $x_3 \vee x_2$ | $(x_3 \vee x_2)x_1x_0$ | $x_1x_0$ |
| 1 | 0 | 1 | | $(x_3 \vee x_2)(x_1 \vee x_0)$ | $x_1 \vee x_0$ |
| 1 | 1 | 0 | | $(x_3 \vee x_2) \vee x_1x_0$ | $x_1x_0$ |
| 1 | 1 | 1 | | $x_3 \vee x_2 \vee x_1 \vee x_0$ | $x_1 \vee x_0$ |

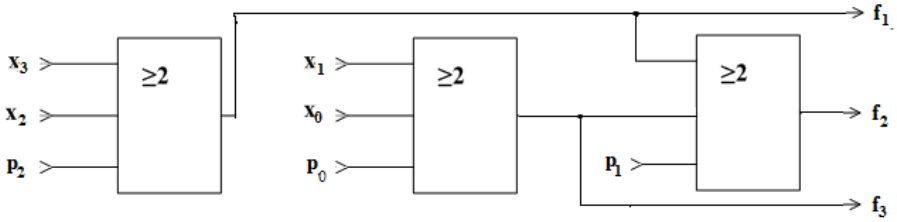



Fig. 5. 7-input majority PNEG

So, 7-input PNEG should have 2-2-AND and 4-AND gates when polirization on programmable input $p_2 = p_1 = p_0 = 0$, and when $p_2 = p_1 = p_0 = 1$, and 2-2-OR and 4-OR gates. Respectively, for polirization 0, 1, 0 we have product of sums $f_2(0,1,0) = (x_3 \vee x_2)(x_1 \vee x_0)$.

## IV. Simulation Results

In designing area of QCA Designer two simulation engines can be used: bistable engine and coherent vector [5]. For simulation of PNEG with 7 inputs and 3 outputs (see Fig. 5), first one is applied. In the bistable engine, each cell is modeled as a simple two-state system. The bistable engine utilized an approximation based in on interection between cells, namely the interaction strength between two cells decaying inversely with the fifth power of the distance separating them. Hence, using this engine, not all cell efects are considered. Only cell effects within an area defined by the so-colled redius of effect *R* are considered for each cell.

Layout of QCA circuit for PNEG with polarization 0, 1, 0 is shown on Fig. 6. care must be taken in partitioning of circuit into clocking zones, which fulfill the scheduling constrain, namely, all signals arrive at their destination simultaneously. Also, it is important that each clocking zone IS of a similar height, so that clock can be easily an uniformly distributed.

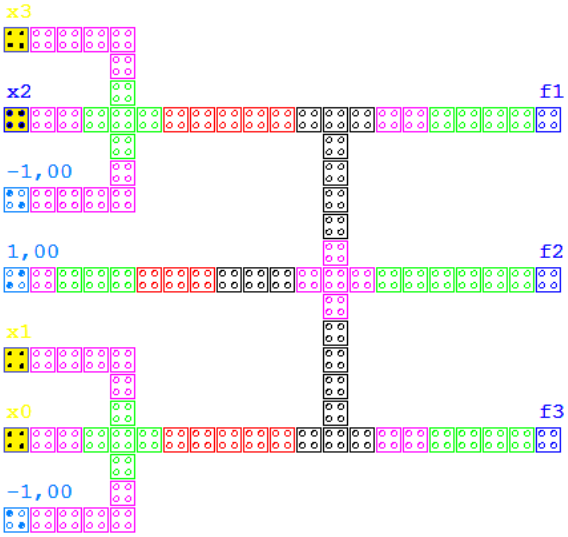



Fig. 6. QCA layout of PNEG for polarization 0,1,0

The simulated layout is based a QCA cell sized 18×18 nm, with 4 quantum dots each having a diameter of 5 nm, and the distance between the center of cells being 20 nm. The total number of cells is 1,0,1 and dimensions of the PNEG design are (420×380) nm. There are 4 information inputs $x_3, x_2, x_1$ and $x_0$, 3 fixed polarized programmable inputs $p_2, p_1$ and $p_0$ and 3 outputs $f_1, f_2, f_3$.

The one possible result of circuit program simulation is shown on Fig. 7.

It is possible to use this PNEG to represent biggest or smaller functions also. For example, this circuit could be used to implement a 3-AND gate or a 3-OR gate by changing one of the information variable inputs into a programmable input, thus increasing the number of programmable inputs by one. Although these smaller functions could be implemented more compactly by other methods, if this PNEG were available, for example in an FPGA implementation, it could also be used in this reduced manner.

Programmable nanoelectronics gates (see Fig. 5) can be programmed for the technical realization logic elements that performed function of two arguments Exclusive OR (XOR) at second output $f_2$:

$$f_{XOR} = \bar{x}_1 x_0 \vee x_1 \bar{x}_0, \quad (5)$$

and Exclusive OR-NOT (XNOR):

$$f_{XNOR} = \bar{x}_1 x_0 \vee \overline{x_1 x_0}. \quad (6)$$

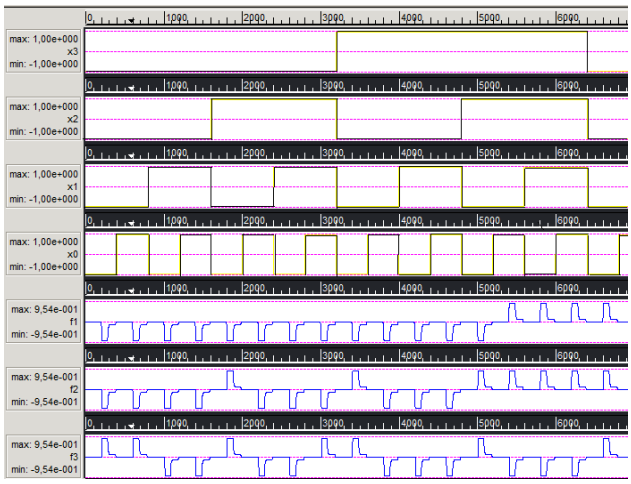


Fig. 7. Simulation waveforms of PNEG for polarizations 0, 1, 0

Really, programmable polarization inputs $p_2 = 0$, $p_1 = 1$, $p_0 = 0$ and performing replacement $x_3 = \overline{x}_1, x_2 = x_0$ and $x_0 = \overline{x}_0$, to minimize the function (5). As of realization of next function (6) at the same polarization, to need replace $x_3 = \overline{x}_1, x_2 = \overline{x}_0$.

Based on PNEG also realized full-adder of two addicate $x_1, x_0$ and carry $C_{\text{in}}$. In this case programmable reducing to replace $x_3 = \overline{x}_1, x_2 = x_0$, $p_2 = p_0 = C_{\text{in}}$, and $p_1 = x_1$. At last two output $f_2$ and $f_3$ of PNEG (see Fig. 5) formed state of sum $S$ and carry in higher bit $C_{\text{out}}$:

$$f_2 = S = maj\left[ maj\left(\overline{x}_1, x_0, C_{\text{in}}\right), x_1, \overline{C}_{\text{out}} \right];$$

$$f_3 = C_{\text{out}} = maj\left(x_1, x_0, C_{\text{in}}\right).$$

## V. Conclusion

This paper presented a 7-input and 3-output PNEG composed from three QCA majority gates. Three of these inputs typically function as programmable inputs to determine the Boolean functions formed by the two and four other inputs to the circuit. This 7-input gate can be configured as a 4-AND gate. A 4-OR gate, a product of sums representation, a sum of products representation, and other variations.

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**О. С. Мельник, Н. В. Трохименко, О. В. Онищук. Наноелектронні логічні елементи**
Описано квантові коміркові наноелектронні автомати з використанням простих логічних мажоритарних елементів. Семивходовий програмований нанопристрій може виконувати функції багатьох логічних елементів, таких як, чотиривходовий логічний елемент І чи чотиривходовий логічний елемент АБО, добутки декількох сум аргументів і декілька сум різних добутків та їх комбінації.
**Ключові слова:** квантовий коміркoвий автомат; мажоритарний елемент; наноелектронні логічні елементи.

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**А. С. Мельник, Н. В. Трохименко, О. В. Онищук. Наноэлектронные логические элементы**

Описаны квантовые сотовые наноэлектронные автоматы с использованием простых логических мажоритарных элементов. Семивходовое программированное наноэлектронное устройство может выполнять функции многих логических элементов, таких как, четырехвходовой логический элемент И или четырехвходовой логический элемент ИЛИ, произведения нескольких сумм аргументов и несколько сумм разных произведений и их комбинации.
**Ключевые слова:** квантовый сотовый автомат, мажоритарный элемент, наноэлектронные логические элементы.

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