COMPUTER SIMULATION OF NANOELECTRONICS ARITHMETIC-LOGIC DEVICES

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This paper presents a quantum dot cellular automata two bit multiplier composed from simple 3-input majority gates and inverters. It is reviewed two different methods of conductors crossing and specifics of QCA devices construction correspondently. The way of device working area partition onto clocking zones is defined. Also it is defined the latency of designed multiplier. Research focuses on the design and simulation of QCA using numerical tools such as the QCADesigner tool.

Keywords: quantum cellular automata, majority gate, quantum full adder, two bit multiplier, clocking zone, coplanar crossing, multi-layer crossing.

Introduction: QCA, is a computing paradigm, in which information is encoded in the electronic charge configuration of a QCA cell built from one or two individual molecules [1].

Orientating pairs of quantum cells so that their relative positions determine their effect on each other. The charge interaction between neighboring cells enables the transmission and processing of information. This is functionally analogous but structurally different from how individual gates in integrated circuits are combined to create arithmetical logic and memory circuitry.

Background

1. Basics of QCA theory. QCA devices consist of a dielectric cell with four quantum semiconductor dots, located in the corners, and two mobile electrons. Their position is only dependent on a finite set of cell-values in the vicinity of defined cell. An isolated cell provides tunneling junctions with the potential barriers. They are controlled by local electric fields that are raised to prohibit electron movement and lowered to allow electron movement. Consequently, an isolated cell can have one of three states. A null state occurs when the barrier is lowered and the mobile electrons are free to localize on any dot. The other two states are polarizations that occur when the barrier is raised, and serve to minimize the energy state of the cell. The state set \( Q \) is always finite and typical \( Q = \{0,1\} \). Probability of cell is in one of polarization state can be correlated with charge density of each quantum dot, and can be found with the help of formula:

\[
p = \frac{\rho_1 + \rho_3 - (\rho_2 + \rho_4)}{\rho_1 + \rho_3 + (\rho_2 + \rho_4)} = \pm 1;
\]

where \( \rho_i \) is charge density every quantum dot of cell.

Fig. 1 shows basic QCA cell, its two possible orientations and polarization of electrons.

![Fig. 1. A single QCA cell and its two possible orientations and polarization (p = ±1)](image)
2. Majority Gate and Invertor. Placing cells next to each other in a line and allowing them to interact we can provide flowing of a data down such wire. There are two methods of wire construction in dependence on 45 degree or 90 degree cell orientation theoretically, but on practice it is difficult to manufactured nano-cells with different orientation.

Different gates can be constructed with QCA to compute various arithmetic and logic functions. The basic logic gates in QCA are the majority gate and invertor (fig. 2.)

![Fig. 2. Majority gate (a) and invertor (b)](image)

The output cell will polarized to the majority of polarization of input cells. The Boolean expression for majority function with inputs $a$, $b$ and $c$ is $maj(a, b, c) = ab + bc + ac$. By fixing the polarization of any one input of the majority gate as logic 0 or logic 1, we obtain AND gate or an OR gate respectively: $a \cdot b = maj(a, b, 0)$, $a + b = maj(a, b, 1)$. Creation of a fixed cell can be done within manufactured process and constant signals do not need to be routed within the circuit.

3. Clocking. Clocking plays a key role in controlling functionality of the QCA logic. This control is accomplished by attaching cells to clocking zones in such way that they latch in succession in the direction of desired signal flow. When potential is low, the electron wave functions become delocalized, resulting in no definite cell polarization. Raising the potential barrier decreases the tunneling rate and thus, the electron begins to localize. As the electron localizes, the cell gains a definite polarization. When the potential barrier has reached its highest point, the cell is said to be latched. Latched cells act as virtual inputs, and as a result, the actual inputs can start to feed in new values. So there is some delay in propagation across QCA cells, unlike for CMOS. In order to have active computation, signals pass through clocking zones, which represent areas where this computation is occurring. The clocking zones are physically adjusted, which means computation must proceed from one to the next in sequential order. Therefore signals should arrive at their destination simultaneously.

For majority gate, its cells should be in a clocking zone separate from clocking zones of the other cells so that majority gate line up on the edges of another clocking zone.


A 1-bit QCA full adder can be assembled from three majority gates and two invertos (fig. 3.). The expressions for the sum and carry output for this adder:

$$S = maj(C_{out}, x_0, maj(x_1, x_0, C_{in})),$$

$$C_{out} = maj(x_0, x_1, C_{in}),$$

where $x_0, x_1, C_{in}$ are the inputs, and $S$ and $C_{out}$ are the outputs.

By connecting a 90 degree cell in the middle of two of these 45 degree cells, both the original input signal (Output 1) and its complement (Output 2) can be obtained. Layout of such construction is shown on fig. 4.
Fig. 3. The schematic diagram of full adder

Fig. 4. Nanowire for simultaneous transmission of original (Output 1) and complement to it (Output 2) signals

On fig. 5. layout of this full adder is shown. For construction of input wires 45 degree cell orientation is used. Performing such implementation gives inverter chain where each cell takes on the opposite polarization of its neighbors. When a wire of regular cells crossovers a wire of an inverter chain (45 degree cells) the two wires do not interact and wires of different type can interact independently on the same fabrication layer. Thus signals can be crossed directly over each other. Such crossing is called coplanar crossing [3; 4]. The problem of coplanar crossing is that distance between cells of single wire lead to low passing of signal.

Fig. 5.QCA full adder layout
The latency for this adder is one clock cycle, consisting of the four clocking zones (which are presented with different color of gray).

5. Multiplier. Design of 2 bit multiplier is rather complicated in comparison with design presented before, which is connected not only with implementation of bigger amount of operation components but also with necessity to layout multiplier in several layers. For such reason, a multi-layer crossing can be used. A tradition multi-layer crossing can be constructed with either cell type, as long as the vertical distance of the wires is large enough to prevent signal leaking from one layer to another, and there is a way to create vias of stacked cells between the layers. Also, because there are propagation delays between cell-to-cell reactions, there should be a limit of the maximum cell count in a clock zone. This ensures proper propagation and reliable signal transmission. The minimum separation between two different signal wires is the width of two cells. This rule should be followed also for transversal wires of different layers, using more than one layer of cells like a bridge. The expressions for outputs of 2-bit multiplier implemented with three input majority gate are:

\[ P_0 = x_0 y_0 = maj(x_0, y_0, 0); \]
\[ P_1 = x_1 x_0 y_1 + x_1 x_0 y_0 + x_1 y_1 y_0 + x_1 y_0 y_0 = \]
\[ = maj(maj(x_0, y_1, 0), maj(x_1, y_0, 0), C_1), maj(maj(x_0, y_1, 0), maj(x_1, y_0, 0), C_1), C_1); \]
\[ P_2 = x_1 y_1 y_0 + x_1 x_0 y_1 = \]
\[ = maj(C_2, maj(C_1, maj(maj(x_0, y_1, 0), maj(x_1, y_0, 0), C_1), maj(x_1, y_1, 0)), \]
\[ \overline{maj}(C_2, maj(maj(x_0, y_1, 0), maj(x_1, y_0, 0), C_1), maj(x_1, y_1, 0)); \]
\[ P_3 = x_1 x_0 y_1 y_0 = maj(C_2, maj(x_1, y_1, 0), M(c_1, maj(x_0, y_1, 0), maj(x_1, y_0, 0)), \]
where \( x_0, x_1, y_0, y_1 \) – input signals, and \( P_0, P_1, P_2, P_3 \) – corresponding bits of output product, \( C_1, C_2 \) – the carries from the previous state.

For circuit layout and functionality checking, a simulation tool for QCA circuits, QCADesiner is used [5] This tool allows users to do a custom layout and then verify QCA circuit functionality by simulations.

Based on previous approaches, a 2 bit multiplier is designed. It consists of two full adders and four majority elements with one fixed polarized input, that made it work like AND gate. Its schematic diagram is presented by fig. 6.

Fig. 6. Schematic diagram of 2 bit multiplier
Layout of QCA circuit is shown on fig. 7. Care must be taken in partitioning of circuit into clocking zones, which fulfill the scheduling constrain, namely, all signals arrive at their destination simultaneously. Also, it is important that each clocking zone IS of a similar height, so that the clock (which is an electric field created under the clocking zone that controls the dot’s state) can be easily and uniformly distributed. The latency for this multiplier is three clock cycles, consisting of the four clocking zones.

The circuit layout is implemented in 6 cell layers to avoid coplanar crossing problems connected with low signal coupling between two wires.

The simulated layout is based on a QCA cell sized $18 \times 18$ nm, with 4 quantum dots each having a diameter of 5 nm, and the distance between the center of cells being 20 nm. The dimensions of the full multiplier design are $1250 \times 820$ nm. There are 6 inputs including conditional carries from previous state, 4 fixed polarized cells and total number of cells is 630, some of which are not visible on shown layout because of the between-layer cells.

Simulation results. In designing area of QCADesigner two simulation engines can be used: Bistable Engine and Coherent Vector Engine [5]. For simulation of a 2 bit multiplier, first one is applied. In the bistable engine, each cell is modeled as a simple two-state system. The bistable engine utilized an approximation based on interaction between cells, namely the interaction strength between two cells decaying inversely with the fifth power of the distance separating them. Hence, using this engine, not all cell effects are considered. Only cell effects within an area defined by the so-called radius of effect $R$ are considered for each cell. Taking this into consideration, it is decided to use multi-layer wire crossing, because radius is not large enough to provide necessary effect of cells of coplanar crossed wires. There is time delay between input signal and appearing of output reaction.
For example, if we take \( x_1 = 0, x_0 = 1, y_1 = 1, y_0 = 0, C_{in1} = 0, C_{in2} = 0 \), which corresponds to time from 2000ns to 2400ns, one can see that, in accordance with the graphs of simulation \( P_3 = 0, P_2 = 0, P_1 = 1, P_0 = 0 \).

The result of circuit program simulation is shown on fig. 8.

![Simulation waveforms of 2-bit multiplier](image)

**Fig. 8.** Simulation waveforms of 2-bit multiplier

**Conclusion.** This paper presented a computer-aided design two bit multiplier composed from four 3-input majority gates with one polarized input (\( p = -1 \)) and two full adders. Usage of multilayer wire crossover permits to avoid coplanar crossing problems. Design is implemented in such way that all outputs were in last four clocking zone which corresponds to phase of relaxation after phase of calculation is being carried out. It is determined that required three full clock cycles are needed for fulfillment of operation of multiplication. The issue to create a reliable leveling of 2-bit multiplier and increasing robustness of circuit is attained. But presence of faults and defects inherent to the molecular technologies requires further work in this direction.

**References**

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Компьютерное моделирование наноэлектронных арифметико-логических устройств

Работа посвящена компьютерному проектированию двухразрядного уникального арифметико-логического устройства на ячейковых квантовых автоматах, в состав которого входят исключительно мажоритарные логические сумматоры и инверторы. Рассмотрены два способа пересечения проводников и соответствующие особенности построения приборов на квантовых ячейковых автоматах. Определены способы деления площади спроектированного умножителя на зоны синхронизации и задержки в срабатывании прибора. Выполнено моделирование квантовых ячейковых автоматов с использованием автоматизированной системы проектирования QCADesiner.