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MODELING OF NANOCIRCUITS WITH PROGRAMMABLE LOGIC

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Abstract—*The design of reliable nanoelectronic circuits with programmable logic based on the technology of quantum automata has been described. While constructing majority circuits of combinational and sequential types the interaction of Coulomb forces using. The order of synthesis and programming of various types of arithmetic-logic devices has been analyzed.*

Index Terms—Quantum nanodots; majority elements; computer-aided design.

I. INTRODUCTION

The contradictions between universatility and specialization can be eliminated through the development of nanocircuit with programmable logic (NCPL), which algorithms of work can be changed at the request of the developer of a particular computer equipment, that is by creating the arithmetic logic circuits with programmable features.

The development of theory and practice of using a majority principle is an urgent problem at present time, because the performance of nanoelectronic computing systems with programmable logic significantly reduces their cost and greatly simplifies the phase of computer-aided circuit design. One programmable nanocircuit replaces from 10 to 10^4 logical gates with medium scale of integration.

II. PROBLEM STATEMENT

The problem of developing the design principles of the reliable computer technology is very important nowadays. Application of mathematical and circuit analysis along with computer-aided design systems can significantly improve the reliability of designing devices.

III. MAIN MATERIAL

The most promising area of nanoelectronics is creation of multi-functional computer systems when one module combines a large number of logic gates into a single functional unit, intended to implement complex logic functions. These electronic and computer systems must satisfy the following basic requirements:

– have a minimum number of external connections;

– have a hardware compatibility;

– use the same type of cells if it is possible;

– have a property extension, that is to have a flexible structure.

To implement electronic systems with variable structure, besides, it needs to be able to programmatically change the technical parameters of the elements during or before work. In terms of cheapening of nanoelectronic systems and improving the reliability of their work they should be performed on the same type of gates with the same configuration of connections between cells.

Programmable nanoelectronic device, which consists of three universal majoritaryn elements (UME), duly connected to each other (Fig. 1), can be used as such cell to build majority programmable systems (PS). Informational $(x_6, x_5, x_4, x_3, x_2, x_1, x_0)$, programmable (p_2, p_1, p_0) signals and intrinsic feedback (f_1, f_2, f_3) are submitted to the inputs of UME [1], [2].

With the help of NCPL of this type all 16 and 65 536 functions of two and four arguments can be implemented, including functions of sum, difference, carry and borrow, functions of one, two and three memory elements, and majority functions of the five or six or seven arguments. The feature of NCPL is that it is logical possibilities and connections may be changed by the program that allows it to be used for constructing of PS. The most important functions in majoritarian and Boolean basis, implemented on the base of NCPL, are shown in Table I.

Nanocircuits with programmable logic is a functionally complete units, because in its composition are functionally complete UME.

Synthesis of majority micro- and nanoelectronic systems on the base of NCPL is recommended to do according to the following order [3].

1. The Boolean functions, which are specified or obtained, are presented in majority basis.

2. The minimization of obtained majority function is performed.

3. The row, which is equivalent to the minimum form of the majority function, is sought in Table I.

4. A block diagram of the given system is created, considering the opportunities of NCPL and specified number of inputs.

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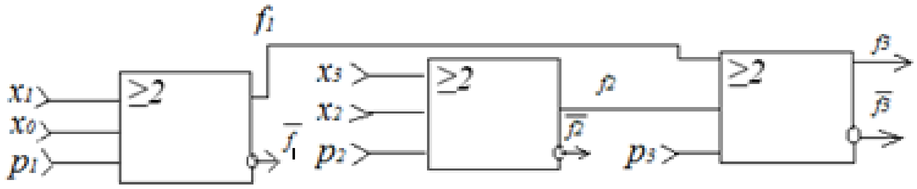


Fig. 1. A universal nanoelectronic device with programmable logic

TABLE 1

THE MOST IMPORTANT FUNCTIONS IN MAJORITARIAN AND BOOLEAN BASIS, IMPLEMENTED ON THE BASE OF NCPL

N	p_1	p_2	p_3	f_1	f_2	f_3	Numbers of output functions
1	0(1)	0(1)	0(1)	$x_1 \cdot x_0$ $(x_1 x_0)$	$x_3 \cdot x_2$ $(x_3 x_2)$	$x_3 \cdot x_2 \cdot x_1 \cdot x_0$ $(x_3 x_2 x_1 x_0)$	$2^3 \cdot 3 \cdot 2^3 = 192$
2	0(1) x_4	(1) x_4, x_5	0(1) x_4, x_5, x_6	$maj(x_1, x_0, x_4)$	$maj(x_3, x_2, x_5)$	$maj(f_1, f_2, x_5)$	$2^3 \cdot 3 \cdot 2^3 \cdot 3 = 576$
3	0(1) f_1, f_2, f_3	0(1) f_2, f_3	0(1) f_3, x_4, x_5	$maj(x_1, x_0, f_1, (f_2, f_3))$	$maj(x_3, x_2, f_2, (f_3))$	$maj(f_1, f_2, f_3)$	$2^3 \cdot 3 \cdot 2^3 \cdot 3 \ldots 2^3 = 4308$

The functioning of the systems on quantum cellular automata (QCA) is based on the interaction of Coulomb forces of quantum dots for performing logic functions. They are designed to reduce the use of CMOS transistors and to solve the problems of density and connection of devices. The cellular automata consists of grouped quantum dots, connected with tunnel junctions and capacitors. Quantum dots are regions of low potential, which are surrounded by a ring of high potential. There are several methods of their formation, but the most common ones is metallization. In cellular automata four quantum dots are placed in the corners of a square. Each automata contains two electrons, which are placed diagonally, because of the action of Coulomb repulsion forces, in opposite corners (Fig. 2). Two possible location of these electrons are marked as polarization of cells $P = -1$ and $P = +1$ [2].

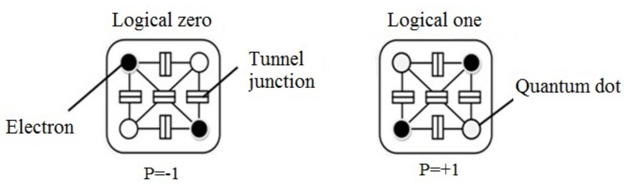


Fig. 2. Quantum cells in states of logical zero and logical one

Placing QCA next to each other in a line and allowing them to interact we can provide flowing of a data down such wire. By connecting a 90 degree cell in the middle of two of these 45 degree cells, both the original input signal (Output 1) and its complement (Output 2) can be obtained. Layout of such construction is shown on Fig. 3.

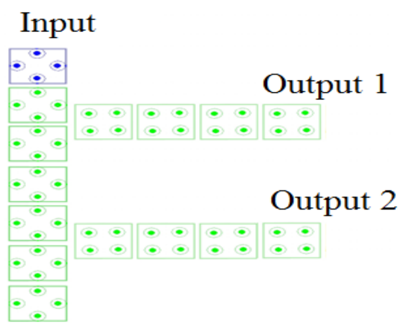


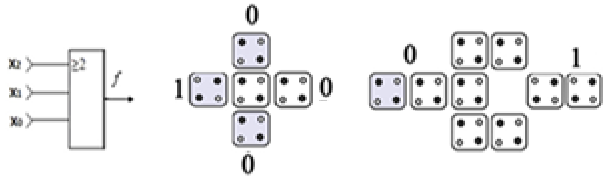
Fig. 3. Nanowire for transmission of original (Output 1) and complement to it (Output 2) signal

Different gates can be constructed with QCA to compute various logic and arithmetic functions. The basic in QCA are the majority element (a) and inverter (b) on Fig. 4.

The output cell polarized to the majority of polarization of input cells. The Boolean expression for majority function with input x_2, x_1 and x_0 is:

$$f = maj(x_2, x_1, x_0)$$

$$= x_2 x_1 \vee x_2 x_0 \vee x_1 x_0.$$



a b

Fig. 4. Majority element (a) and inverter (b) in QCA

By fixing the polarization of any one input of the majority gate as logic 0 or logic 1, we obtain AND gate or an OR gate respectively:

$$f_{\mathrm{AND}} = maj\left(x_2, x_1, 0\right) = x_2 \vee x_1,$$

$$f_{\mathrm{OR}} = maj\left(x_2, x_1, 1\right) = x_2 \vee x_1.$$

Clocking plays a key role in controlling functionality of the QCA logic. This control is accomplished by attaching cell to clocking zones in such way that they in succession in the direction of desired signal flow. When potential is low, the electron wave function become delocalized, resulting in no definite sell polarization. Raising the potential barrier decreases the tunneling rate and thus, the electron begins to localize. As the electron localizes, the cell gains a definite polarization. When the potential barrier has reached its highest point, the cell is said to be latched. Latched cell act as virtual inputs, and as a result, the actual inputs can start to feed in new values. So there is some delay in propagation across QCA cell, unlike for CMOS. In order to have active computation, signal pass through clocking zones, which represent areas where this computation is occurring. The clocking zones are physically adjusted, which means computation must proceed from one to the next in sequential order. Therefore signals should arrive at their destination simultaneously.

In Table I $x_6, x_5, x_4, x_3, x_2, x_1, x_0$ are input informational signals, represented either in direct or inverse code; p_2, p_1, p_0 are programmable signals; f_1, f_2, f_3 are output signals of correspond UME.

Let us synthesize the function of logical adding of four arguments, using computer-aided design system QCADesigner [4]:

$$f_3 = x_3 \vee x_2 \vee x_1 \vee x_0, \tag{1}$$

which corresponds to the Boolean equivalent in the first row in Table I.

Functions of logical addition of two of the four arguments are formed on two additional outputs of NCPL:

$$f_1 = x_1 \vee x_0 = maj\left(x_1, x_0, 1\right), \tag{2}$$

$$f_2 = x_3 \vee x_2 = maj\left(x_3, x_2, 1\right). \tag{3}$$

IV. SIMULATION RESULTS

To program the functions (1), (2) and (3) the programmable inputs must be set in the polarizations $p_1 = p_2 = p_3 = 1$ in block diagram of NCPL (see Fig. 1).

The Figure 5, a shows a block diagram of NCPL, which is built on the working field of QCA Designer. It consists of 55 quantum cells, which have size (18×18) nm, with 4 quantum dots about 5 nm in diameter 20 nm distance between their centers. The total size of NCPL is (198×318) nm^2. It has four informational inputs x_3, x_2, x_1 and x_0, three programmable inputs p_1, p_2, p_3 with polarizations $+P = 1$ and three pairs of complementary outputs f_1, f_2 and f_3.

The results of computer-aided design of NCPL waveforms are shown on Fig. 5,b. Positive pulses correspond to positive polarizations + P = 1, and negative – negative polarizations $-P = 0$. The corresponding truth table of NCPL for this programming mode is shown in Table II.

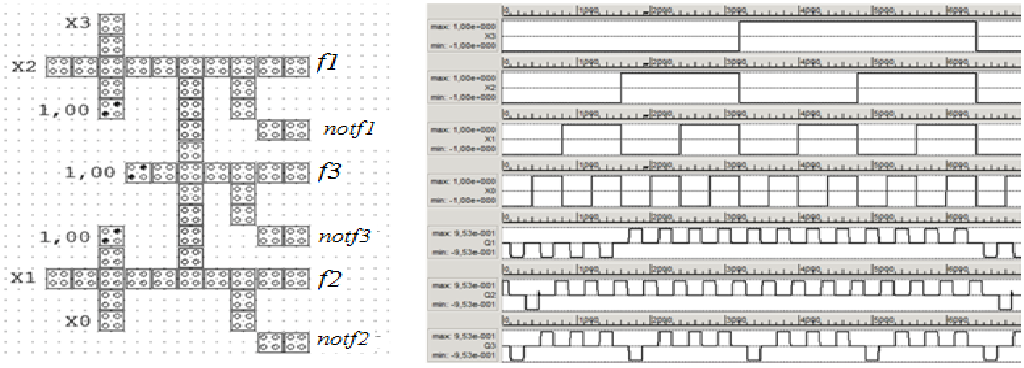
With the change of polarization of the inputs p_1, p_2, p_3 NCPL with seven inputs (see Fig. 1) can be programmed for 5376 logical functions of two and six inputs combinational circuits. For example, for the first version of the programming $p_1 = p_2 = p_3 = 0$ synthesized elements of logic multiplication: $f_1 = x_1 x_0$, $f_2 = x_3 x_2$, $f_3 = x_3 x_2 x_1 x_0$.

Sum of pairwise products of the four arguments $f_2 = x_3 x_2 x_1 x_0$ implemented in the first raw of Table I, and product of pairwise sums $f_3 = (x_3 \vee x_2)$ $\cdot(x_1 \vee x_0)$ – in the second. Now lets synthesize the circuit for the third raw of the Table I, which consists of two RS-triggers with separate inputs x_3, x_2 and x_1, x_0, covered with feedbacks $p_1 = f_1$ and $p_2 = f_2$. Direct outputs f_1 and f_3 of these triggers are combined into third majority element (see Fig. 1), which in this case implements operation of logical multiplication $maj\left(f_1, f_2, 0\right)$. On Figure 6, a built this sequential nanoelectronic circuit in the form of QCA Designer, and the results of time simulation are shown on Fig. 6,b. It has a size (258×338) nm^2 and consists of 81 quantum automatas.

Verification table of sequential NCPL states are given in Table III.

V. CONCLUSION

In the nearest ten years microelectronic components of circuits with high scale integration will achieve quantum technological limitations and will not meet the increasing performance requirements of computer technology. Therefore, new nanotechnologies are developing so actively, that would provide significantly higher performance. One of such developments is the quantum cellular automata and created on its basis systems with programmable logic. As shown above, such devices will provide realization of full system of logic functions for both combinational and sequential arithmetical and logical computing devices.



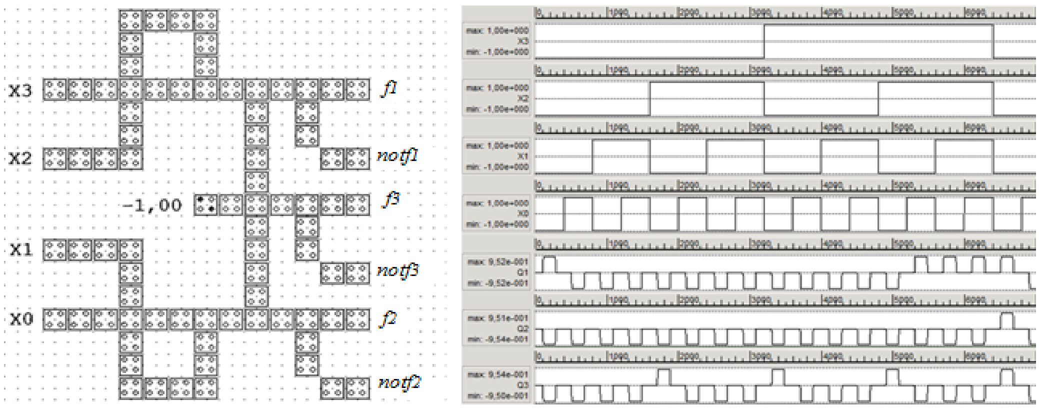
a b

Fig. 5. Computer-aided design of combinational NCPL on QCA

TABLE II

TRUTH TABLE OF FUNCTIONS $maj(x_3, x_2, 1)$, $maj(x_3 \vee x_2, x_1 \vee x_0, 1)$ AND $maj(x_1, x_0, 1)$

x_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
x_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
x_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
x_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
f_1	0	0	0	0	1	1	1	1	0	1	1	1	1	1	1	1
f_2	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
f_3	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1



a b

Fig. 6. Computer-aided design of sequential NCPL on QCA

TABLE III

TRUTH TABLE OF FUNCTIONS $maj(maj(x_3, x_2, f_2), maj(x_1, x_0, f_1), 0)$

x_3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
x_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
x_1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
x_0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
f_1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
f_2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
f_3	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

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О. С. Мельник, В. Т. Гірняк. Моделювання наносхем з програмованою логікою

Реалізовано комп’ютерне моделювання наноелектронних схем з програмованою логікою на базі технології квантових коміркових автоматів. Під час проектування мажоритарних схем комбінаційного та послідовністного типів використовувалась теорія взаємодії кулонівських сил. Проаналізовано порядок побудови та програмування деяких типів логічних та тригерних пристроїв.

Ключові слова: квантові наноточки; мажоритарний елемент; автоматизоване проектування.

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А. С. Мельник, В. Т. Гирняк. Моделирование наносхем с программируемой логикой

Реализовано компьютерное моделирование наноэлектронных схем с программированной логикой на базе технологии квантовых сотовых автоматов. При проектировании мажоритарных схем комбинационного и последовательностного типов использовалась теория взаимодействия кулоновских сил. Проанализирован порядок построения и программирования некоторых типов логических и триггерных устройств.

Ключевые слова: квантовые автоматы; мажоритарные элементы; автоматизированное проектирование.

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